650iMQ **16** %S%C%H%^%$%/%m%W%m%;%C%5 **PICO-**

@>B< 9n?.　　9)F# CN9(　　E7Ln 1Q@2

7DXf5A=NBg3X M}9)3XIt　　El5~9)2JBg3X 9)3XIt　　7DXf5A=NBg3X M}9)3XIt

%O!<%I%&%'%"5-=R8@8l **(SFL)** $H=q$-49$(2DG=$J%2!<%H%"%l%$ **(FPGA)** $rMQ$$$k3HKh$j!"%^%$%/%m%W%m
$N@_7W$+$iF0:n3NG'$^Gr0l4S7F9TJ&650iMQ$N%^%$%/%m%W%m%;%C%5<B83%7%9%F%`$N9=@.$H!"3l$r<B:
BP>]$K9T$JC?<B83$N<B;\Nc$K$D$$$F=RYk!#K\%7%9%F%`$O!"0lEY$K$"$kDxEYB?$/$N3X@8$rBP>]$H7?<B8
3H$r2DG=$K9kbN$G!"Hf3SE*0B2A$K<B8z@-$N9b$$<B83$r<B8=$9k3H,G-$k!#

1　O8aK

Bg3XK*1k7W;;5!650iK*$$$F!"%3%s%Q%$%i/%"%s%V
%iEy$N%=%U%H%&%'%"!"7W;;5!%"!<%-%F%/%A%c!"LSI @_7W$N0l
4S650i$O!"3X@8$K9-$/<B:]E*$JCN<1$H7P83$rM?$($k$H6&$K!"
AOBNOr;I7c$7!"7W;;5!$KBP9k6=L#$r9b$a$kE@$GHs>o$KM-
8zG"$k [1]!#

3Nh&$J!"0l4S650i$N80HJkN$O!"@_7WBP>]$HJk$9
0iMQ%W%m%;%C%5$N<B8=$G$"$k!#=>Mh!"650iMQ%W%m%;%C%5$O
40A4$J%Z!<%Q%^%7%s$G%7%_%e%l!<%?>eGN$_F0:n$9kb$N
$,B?$+C?$,!"6aG/!"@_7WMQ%D!<%k$NIa5Z!"=q-49(2DG=$J
%2!<%H%"%l%$ (FPGA) $N=8@QEY$N8~>eJIKh$j!"Bg3X$K
$*$1$k<B83650i4D6-$,@0Hw5lkH6&$K!"<B:]$K650iMQ%W%m
%;%C%5$r@=:n$9$k<B83$K$D$$$F$NJs9p$,3hH/KJjDD"$k
[2][3][4][5]!#

:#$^$G$KJs9p$5lF$?;n$_NCfG!"6e=#Bg3XK*1k Kue-
Chip[2], QP-DLX[3]!"6e=#9)6HBg3X$N Kite[4] $O!"L?Na%;%C
%H$,7h$^CF$$$k650iMQ%W%m%;%C%5G"$k!#3X@8$O650i$N<1
4|CJ3,GO!"4{$K<BAu$5lF$?%A%C%W$N%b%K%?5!G=$rMQ$$$F
$=$NF0:n$r2r@O$7!"L?Na<B9T;~$N CPU $NF0:n$K$D$$$F$NM}
2r$r?<$a$k!#$5iK!"%3%s%H%m!<%i$N@_7W!"%Q%$%W%i%$%s
M}Ey$N9bB.2=!"LSI %A%C%W$X$N<BAu$rDL8F%"!<%-%F%/%A%c

$NMM!9$J%l%Y%k$N@_7W5;=Q$H LSI @_7W<BAu5;=Q$r=,F@$9$
%A%C%W$N3+H/$O<B:]$N%2!<%H%"%l%$$r:n@.9k3H$,M}A
$,$k$V!"FPGA $rMQ$$$F$b!"F0:n$N3NG'!"%W%m%0%i%`$N<B
$,2DG=$G$"$k!#F1;~$K%"%;%s%V%i/%3%s%Q%$%i$N:n@.$r9
$J!"%=%U%H%&%'%"%l%Y%k$N@_7W5;=Q$r=,F@$9$k!#
0lJ}!"El5~Bg3XM}3XIt>pJs2J3X2JGO!"40A4$KL?Na%;%C
%G!<%?%Q%9$r40A4$K3X@8KBP7$F%*!<%W%s$K7F!"CPU
$r<+M3$K@_7W5;$k<B83$r;n$_$F$$$k!#3X@8$O<+J,$G9M$($?L?Na%;%C
%H$r@_7W$9k3HG!"CPU $r@_7W$7!"FPGA >e$
$K<BAu$9kH6&$K!"$3$NL?Na%;%C%H$KBP9k%"%;%s%V%i/%3%
%Q%$%i$N:n@.$r%W%m%0%i%_%s%0<B83$G9TJ&!#:G=*E*KO!
3N%9%l!<%7%s%0$N%W%m%0%i%`$r<B9T$7!"$=$NF0:nB.EY$rB
$N%W%m%;%C%5$i!"@_7WK*1k%l!<%I%*%U$K4X$7$FBN83$9$k[
A0<T$NJ}K!$O!"=i4|CJ3,GN650i$r8z2LE*$K9TJ&3H
G-kH6&$K!"%F%-%9%HEy$N:n@.$,MF0W$G!"$"$kDxEYBg?
$rBP>]$H9k3H$,2DG=$@$,!"650i$N$+$J$j@h$NCJ3,K
$J$$$H!"3X@8$NAO0U$r9kItJ,$,=P$F3J$$798~K"$k!
J}!"8e<T$NJ}K!$O$[$\7W;;5!650i$NM}A[$K6a$$$,!"A4BN$
$FB?Bg$J;~4VrMW7!"B??M?t$rBP>]$H9k3H$,Fq$7$$$
$+$iB?$/$N;dN)Bg3XGOF3F~$,:$FqG"$k!#
$=$3GO!"N><T$NCf4VE*$JJ}K!!"9JoA!"%G!<%?%Q%9$N
N/$N%c$r;XDj7F!"L?Na%;%C%H$O%*!<%W%s$K7?650iMQ%W

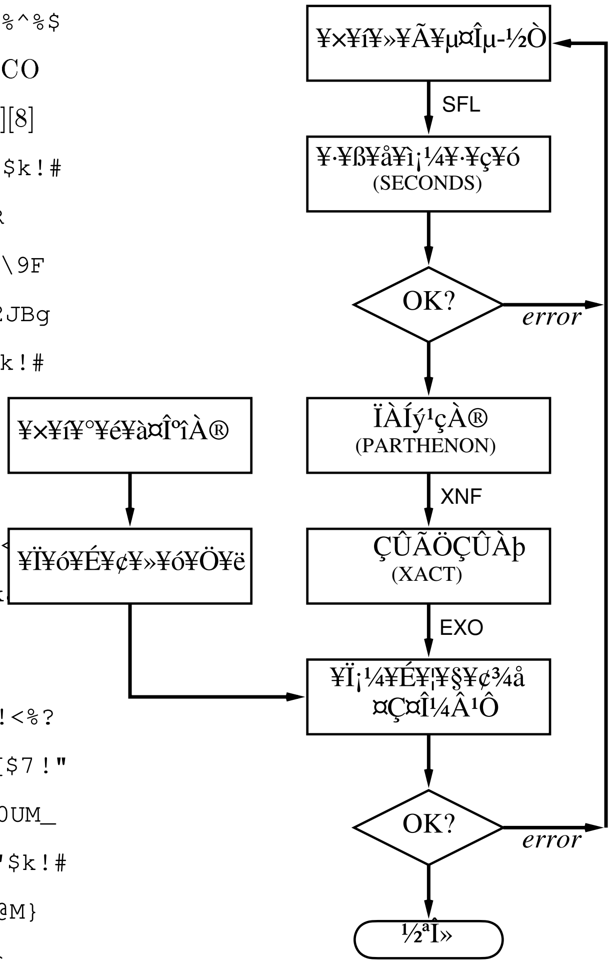
%;%C%5Kh$k<B83$r9TJC$F$$$k [?] !#2f!9O3$N650iMQ%^%$ %/%m%W%m%;%C%5%U%l!<%`%o!<%/$r PICO $H8F$s$G$$$k!#PICO $N3X@8<B83$G$O!"$^$:!"%O!<%I%&%'%"5-=R8@8l SFL[6][7][8] $rMQ$$$F$=$l$>$l$NL?Na%;%C%H$r;}$C$? PICO $r5-=R$9$k!# <!$K PARTHENON[6] $K$h$jO@M}9g@.$r9T$J$$!"Xilinx <R $N FPGA $rMQ$$$?%F%9%H%\!<%I>e$GF0:n$r3NG'$9$k!#K\9F $G$O PICO $N%U%l!<%`%o!<%/!"5-=RNc$r>R2p$7!"El5~9)2JBg 3X$*$h$S7DXfBg3X$G9TJC$?3X@8<B83$K$D$$$FJs9p9k!#

2 3+H/<B83$NOHAH

%^%$%/%m%W%m%;%C%53+H/<B83$O!"<B83N?aNHqMQ!"< ;~4V!"3X@8$N3X=,%l%Y%k$K$*$$$FMM!9$JF3F~7ABV$r<h$k $,$G$-$k$,!"6&DL$7$F0J2<$N%9%F%C%WrH$k!#

- %O!<%I%&%'%"5-=R8@8lKh$k5-=R$r:G=i$K65$(!"%G!<%? %Q%9KD$$$F5-=R5l$?%U%!%$%k$r3X@8$K$^$:G[I[$7!" 3X@8$O3l$r%Y!<%9$H7F@_7W$r9T$J$&!#$bAm$s0UM_ N"$k3X@8$,%G!<%?%Q%9$rJQ99$9k3HO<+M3G"$k!# 8=:_!"%O!<%I%&%'%"5-=R8@8lKO NTT $,3+H/$7$?O@M} 9g@.%7%9%F%` PARTHENON $N5-=R8@8l$G$"$k SFL $r MQ$$$F$$$k!#O@M}@_7W$N<B83$HAH$_9g$o$;$k>l9g!"%2!< %H%l%Y%kGN@_7W$r9T$Jo;k3Hb2DG=$@$,!"%O!< %I%&%'%"5-=R8@8l$rMQ$$$?J}$,!"%O!<%I%&%'%"5-=R8@8l $rA4$/CNiJ$$3X@8$rBP>]$H7?>l9gGb!"Ok$+$K $J$$<B83;~4V$G%^%$%/%m%W%m%;%C%5$r:n@.$9$k3$H$,$G $-$k!#
- L?Na%;%C%H$N9=@.$O3X@8$KG$$;k,!"%G!<%?%Q%9$,4pK\ E*$K7h$^$C$F$$$k$?$a!"$"$kDxEY$N@)8B$r<u1k!#4pK\ E*KO Load/Store 7?$N RISC %"!<%-%F%/%A%c$KJk!# <B83;~4V!"3X@8$N3X=,%l%Y%k$KhCFO!"L?Na$N%3!< %G%#%s%0$NOHAH$rM?$(!"BeI=E*$JL?Na$N5-=RrNcH7F M?$($k3HbG$-$k!#
- %O!<%I%&%'%"5-=R%l%Y%kGN%7%_%e%l!<%7%g%sr-As $H9T$J$$!"3N;~E@$G650w$^$?$O T.A. $NA0$GF0:n$N3N G'$r9TJ&!#
- O@M}9g@.7?2sO)$r FPGA >e$G<B8=$7!"4JC1$J%W%m%0 %i%`$r%O%s%I%"%;%s%V%k$7!"<B9T9k!#

3N%^%$%/%m%W%m%;%C%53+H/<B83$NN.lr?^ 1$K<(



?^ 1: <B83$NN.$l

<B83$G:n@.$9$k%^%$%/%m%W%m%;%C%5$N5,LO$O=c?h$K<B83 M=;;$KhC$F7h$^$j!"3X@8$N%l%Y%k$d<B83;~4V$N1F6A$r< OJ$$!#3lKBP73X@8$N4pACCN<1$,=i4|$NCJ3,$G$"$C$?$ <B83;~4V$,>/$J$$>l9g$O!"L?Na%;%C%H$N%3!<%G%#%s%0Nc$ $($?$j!"$$$/D+$NL?Na$N5-=RrNcH7FM?$($k3HK $F<B83;~4V$rC;=L9k3H$,$G$-$k!#

1993 G/EY!"7DXf5A=NBg3XK*$$$F FPGA $K Xilinx <R$N XC3000 %7%j!<%:$rMQ$$$F 8bit %W%m%;%C%5$r:n@.$9$k;n9T< 83$r9TJC$?!#$=lr85$K!"1994 G/EY$+iOF1 XC4000 %7 %j!<%: [9] $rMQ$$$? 16bit %W%m%;%C%5$N:n@.<B83$r7DXf5A= Bg3X$HEl5~9)2JBg3X$G9TJC$F$$$k!#

3 %^%$%/%m%W%m%;%C%5 PICO

<B83MQ%^%$%/%m%W%m%;%C%5 PICO $O bit scalable — D^ $j!"F1MM$N9M$(J}$G 4bit $+$i 16bit $^$G!"MM!9$J%5%$%:$ <hk3HNG-$k%^%$%/%m%W%m%;%C%5$N%U%l!<%`%o!<%/$ FPGA $N%5%$%:$K1~$8$FL?Na%;%C%H$r9=C[9k3H$,$G$-$

<B83650iMQG"k?$a!"L?Na%;%C%H$OMM!9$J%P%i%(%F%#$ 5v9,!"4pK\J}?K$O0J2<$NDLjG$"$k!#

- RISC G"$k!#$9Jo$AC10lL?NaD9!"Load/Store %"!<%-%F%/%A%cG"$k!#
- %l%8%9%??t$O2DG=$J8B$jB?$/<h$k!#
- %"%I%l%C%7%s%0%b!<%I$O%l%8%9%?4V@\$r4pK\$H9k!#3X @8$N6=L#$Khj!"%G%#%9%W%l!<%9%a%s%HIU$-!"%]%9%H%$ %s%/%j%a%s%H/%W%j%G%/%j%a%s%H!"%$%s%G%C%/%9=$>~$J IrIU1/o(k3H,G-$k!#
- %G!<%?%Q%9$OM=$a7hail?bN$rMQ$$$k!#

8bit L$K~$N9=@. (PICO-4/PICO-5) $O!"FPGA $N5,LO$, ITB-9k;~Kd$`$rF@$:MQ$$$k$b$N$G$"$j!"4pK\E*$K5!3# 8l$rD>@\%a%b%j$KF~$l$FF0$+$7$F$_$k%*%b%A%cDxEY$G$"$k!# 8bit 9=@. (PICO-8) $b4JC1$G$O$"$k$,!"%"%;%s%V%i$r:n$C$F B?>/$N%W%m%0%i%`$rF0$+$9$3$H$,$G$-$k!#%3%s%Q%$%i!"%"%W %j%1!<%7%g%s$r7kSIU1$?0l4S650i$K$O!"$dOj 16bit 0J>e $N9=@. (PICO-16) $,I,MW$G$"$k!#

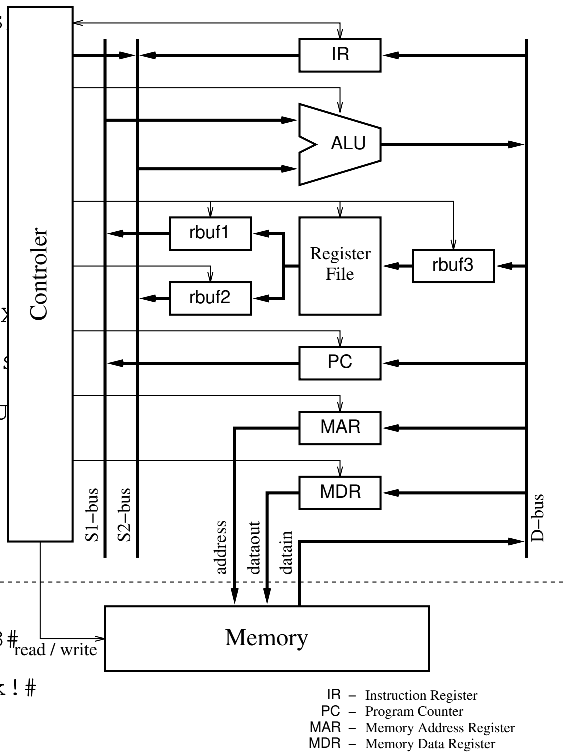
3.1 PICO-16 $N%G!<%?%Q%9

?^ 2$K PICO-16 $N%G!<%?%Q%9$r<($9!#%G!<%?%Q%9>e$K$* 1k4pK\E*$JA`:n$O!"%l%8%9%?%U%!%$%k$+iN%*%Z%i%s%IFI- $_$@$7!"ALU GN1i;;<B9T!"$=7F%l%8%9%?%U%!%$%kXN 7k2L$N=q$-9~$_G"$k!#

%l%8%9%?%U%!%$%k$O 8words×16bits $N RAM $H!"=PNO%P%C %U%!MQ$N%l%8%9%? (rbuf1!"rbuf2) $HF~NO%P%C%U%!MQ%l%8%9%? (rbuf3) $+$i9=@.5l$k!#$3$l0J30$K!"%W%m%0%i%`!&%+%&%s%? (PC)!"L?Na%l%8%9%? (IR)!"$*$h$S30It%a%b%j$r%"%/%;%9$9 k?aN%a%b%j!&%"%I%l%9!&%l%8%9%? (MAR)!"%a%b%j!&%G!< %?!&%l%8%9%? (MDR) $H8F$Plk%l%8%9%?$,B8:_$9$k!#$3$l iO!"FbIt%P%9$r2p$7FDJ,CF$*$j!"$=l>$l S1-Bus!" S2-Bus!"D-Bus $H8F$Plk!#%=!<%9!&%P%9 (S1-Bus!"S2-Bus) $+$i%G%9%F%#%M!<%7%g%s!&%P%9 (D-Bus) XNM#0l$N7PO)$O ALU 7PM3G"$k!#

3.2 PICO-16 $NL?Na%;%C%HNc

3X@8$N3X=,CJ3,$,@u$$>l9g!"$^$?$O<B83;~4V$,ITB-9k>l 9g!"$"$kDxEY$NL?Na$NOHAH$rM?$(kI,MW,$"$k!#3N>l9g!" 0J2<Nh$&$J;X?K$rM?$($k!#



?^ 2: %G!<%?%Q%9

- L?Na$O!"%$%_!<%G%#%($%H$rHkL?Na72H=$l0J30$+ 9=@.5l$k!#
- L?NaD9$N@)Ls$Khj%*%Z%i%s%I$O 2 D^$G!#
- %$%_!<%G%#%($%H$r<h$kL?Na$O!"L?NaD9$NH>J,$r%$%_ %G%#%($%HNN0h$KMQ$$$k!#

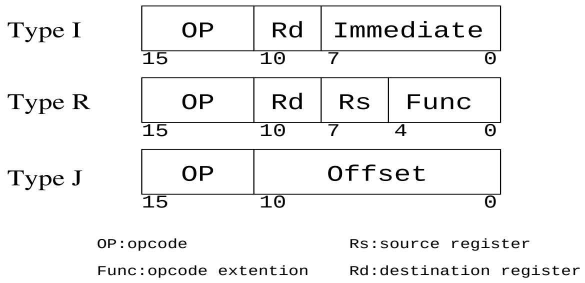
3Nh&$JOHAH$rM?$($?>l9g!"L?Na%;%C%H$O DLX %"!<%- %/%A%c$K6a$/$J$j!"Hennessy & Patterson[10] $r<x6H$N%F%- %9%H$KMQ$$$F$$$k>l9g$O!"$3lH7kSIU1$FM}2r$,MF0W Ok!#

0J2<!"650i<B83MQ$K@_7W$7$? PICO-16 $NL?Na%;%C%H$r< $9!#>l9g$KhCFOL?Na7A<0$N35N,$r<(7?$j!"L?Na$N5 Nc$r$$$/D+<($9$3HKhj!"3X@8KHC+$+$j$rM?$($ H,G-$k!#

3.2.1 L?Na7A<0

9YFNL?Na$O 16 %S%C%HD9$G!"5 %S%C%H$NL?NaA`:n%3!< $rM-$7$F$$$k!#L?Na7A<0$O I(*Immediate*) 7?L?Na, R(*Register–register*) 7?L?Na, J(*Jump*) 7?L?Na$N 3 <oN`$G$"$k!#3l$r?^ 3$K<($9!#

I 7?L?Na$O%m!<%I/%9%H%"!"B(CM1i;;$JIK;HMQ9k!#R L?Na$O;;=QO@M}1i;;$JIK;HMQ$7!"L?NaA`:n%3!<%I$NB>



?^ 3: L?Na7A<0

%U%!%s%/%7%g%s%3!<%I$rM-$7$F$$$k!#J 7?L?Na$OJ,4t (%8%c %s%W) L?Na$*hS>r7oJ,4t (%V%i%s%A) L?Na$K;HMQ$9$k!#L?Na D9$N@)8BKh$j%l%8%9%??t$O R0 $+$i R7 $^$G$N 8 DHJk!# 2 %*%Z%i%s%I L?Na$rMQ$$$F$$$k3H$r=|$-!"$[$\ DLX H 8?L?Na%;%C%HHJCF$$$k!#

PICO-16 $NL?Na%;%C%H$K$O%m!<%I/%9%H%"!";;=QO@M}1i;;!" Hf3S!"@)8f$N 4 DN%?%$%W$,$"$k!#

3.2.2 %m!<%I/%9%H%"L?Na

LDL(Load Low Immediate) L?Na$O%l%8%9%?$N2<0LH>J,$r CM$rBeF~$7!">e0LH>J,$K 0 $r@_Dj$9$k!#$^$?!"LDH(Load High Immediate) L?Na$O%l%8%9%?$N>e0LH>J,KCMrBeF~9k!#$3 lKhj 16 %S%C%HDj?t$N@_Dj$O 2 L?Na$G9T$($k!#

L?Na	7A<0	0UL#
LDL	Rd, #imm	Rd $\leftarrow$ 0^8 ## $\mathtt{imm}_{7..0}$;
LDH	Rd, #imm	Rd $\leftarrow$ $\mathtt{imm}_{7..0}$ ## $\mathtt{Rd}_{7..0}$;
LD	Rd, (Rs)	Rd $\leftarrow$ M[Rs];
ST	(Rd), Rs	M[Rd] $\leftarrow$ Rs;
MOV	Rd, Rs	Rd $\leftarrow$ Rs;

I= 1: %m!<%I/%9%H%"L?Na

3.2.3 ;;=QO@M}1i;;L?Na

9YFN;;=QO@M}1i;;$O%l%8%9%?–%l%8%9%?4V$*hS%l%8%9 %?–B(CM4VN_2DG=G"$k (%m!<%I/%9%H%"!&%"!<%-%F%/%A%c)!# L?NaKO2C;;!"8:;;!"O@M}@Q!"O@M}OB!"GSB>E*O@M}OB!"%7%U %H$,$"$k!#B(CM7A<0$G$O 16 %S%C%H$K 0 3HD%5l$?B(CM$,MR MQG-$k!#

L?Na	7A<0	0UL#
ADDI	Rd, #imm	Rd $\leftarrow$ Rd + (0^8 ## $\mathtt{imm}_{7..0}$);
SUBI	Rd, #imm	Rd $\leftarrow$ Rd - (0^8 ## $\mathtt{imm}_{7..0}$);
ANDI	Rd, #imm	Rd $\leftarrow$ Rd & (0^8 ## $\mathtt{imm}_{7..0}$);
ORI	Rd, #imm	Rd $\leftarrow$ Rd | (0^8 ## $\mathtt{imm}_{7..0}$);
XORI	Rd, #imm	Rd $\leftarrow$ Rd ^ (0^8 ## $\mathtt{imm}_{7..0}$);
SLLI	Rd, #imm	Rd $\leftarrow$ $\mathtt{Rd}_{15-\mathtt{imm}..0}$ ## $0^{\mathtt{imm}}$;
SRLI	Rd, #imm	Rd $\leftarrow$ $0^{\mathtt{imm}}$ ## $\mathtt{Rd}_{15..\mathtt{imm}}$;
SRAI	Rd, #imm	Rd $\leftarrow$ $(\mathtt{Rd}_{15})^{\mathtt{imm}}$ ## $\mathtt{Rd}_{15..\mathtt{imm}}$;
ROLI	Rd, #imm	Rd $\leftarrow$ $\mathtt{Rd}_{15-\mathtt{imm}..0}$ ## $\mathtt{Rd}_{15..16-\mathtt{imm}}$;
RORI	Rd, #imm	Rd $\leftarrow$ $\mathtt{Rd}_{\mathtt{imm}-1..0}$ ## $\mathtt{Rd}_{15..\mathtt{imm}}$;
ADD	Rd, Rs	Rd $\leftarrow$ Rd + Rs;
SUB	Rd, Rs	Rd $\leftarrow$ Rd - Rs;
AND	Rd, Rs	Rd $\leftarrow$ Rd & Rs;
OR	Rd, Rs	Rd $\leftarrow$ Rd | Rs;
XOR	Rd, Rs	Rd $\leftarrow$ Rd ^ Rs;
SLL	Rd, Rs	Rd $\leftarrow$ $\mathtt{Rd}_{15-\mathtt{Rs}..0}$ ## $0^{\mathtt{Rs}}$;
SRL	Rd, Rs	Rd $\leftarrow$ $0^{\mathtt{Rs}}$ ## $\mathtt{Rd}_{15..\mathtt{Rs}}$;
SRA	Rd, Rs	Rd $\leftarrow$ $(\mathtt{Rd}_{15})^{\mathtt{Rs}}$ ## $\mathtt{Rd}_{15..\mathtt{Rs}}$;
ROL	Rd, Rs	Rd $\leftarrow$ $\mathtt{Rd}_{15-\mathtt{Rs}..0}$ ## $\mathtt{Rd}_{15..16-\mathtt{Rs}}$;
ROR	Rd, Rs	Rd $\leftarrow$ $\mathtt{Rd}_{\mathtt{Rs}-1..0}$ ## $\mathtt{Rd}_{15..\mathtt{Rs}}$;

I= 2: ;;=QO@M}1i;;

3.2.4 Hf3SL?Na

Hf3SL?Na$O!"2 DN%l%8%9%?$NHf3S (== , != , > , < , <=) $r9T$&!#Hf3S7k2L$,56 (false) NH$-%G%9%F%#%M!< %7%g%s!&%l%8%9%? (Rd) KO 0 $,@_Dj$5$l!"?? (true) NH$- 0x0001 NCM,@_Dj5l$k!#

L?Na	7A<0	0UL#
SEQ	Rd, Rs	if (Rd == Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};
SNE	Rd, Rs	if (Rd != Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};
SGT	Rd, Rs	if (Rd > Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};
SLT	Rd, Rs	if (Rd < Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};
SGE	Rd, Rs	if (Rd >= Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};
SLE	Rd, Rs	if (Rd <= Rs) Rd $\leftarrow$ 1^{16} else Rd $\leftarrow$ 0^{16};

I= 3: Hf3SL?Na

3.2.5 @)8fL?Na

%W%m%0%i%`$N@)8f$O%8%c%s%WL?Na$H%V%i%s%AL?Na$GJ5 $k!#%8%c%s%WL?Na$O%G%9%F%#%M!<%7%g%s!&%"%I%l%9$N;XD $H%j%s%/$NM-L5$N0c$$$KhC$F 4 DKJ,1ilF$$$k!#

- J!"JAL L?Na$OId9fIU$- 11 %S%C%H!&%G%#%9%W%l!<%9%a% %H$,%W%m%0%i%`%+%&%s%?$K2C;;5l$k!#
- JR!"JALR L?Na$O%8%c%s%W@h$N%"%I%l%9$,3JG<$5lF$ $k%l%8%9%?$r;XDj9k!#

- JAL!"JALR L?Na$O%j%?!<%s%"%I%l%9$r R7 $K3JG<$9$k(<j B3$-8F$S=P$7$G;H$&)!#

- BEQZ!"BNEZ L?Na$O R7 $H 0 $NHf3S7k2L$Khj!"Id9fIU $-11 %S%C%H!&%G%#%9%W%l!<%9%a%s%H$,%W%m%0%i%`%+%& %s%?$K2C;;5l$k!#

L?Na	7A<0	0UL#
J	disp	PC ← PC + $((\mathtt{disp}_{10})^5$ ## $\mathtt{disp}_{10..0})$;
JR	Rd	PC ← PC + Rd;
JAL	disp	R7 ← PC;
		PC ← PC + $((\mathtt{disp}_{10})^5$ ## $\mathtt{disp}_{10..0})$;
JALR	Rd	R7 ← PC;
		PC ← PC + Rd;
BEQZ	disp	if (R7 == 0)
		PC ← PC + $((\mathtt{disp}_{10})^5$ ## $\mathtt{disp}_{10..0})$;
BNEZ	disp	if (R7 != 0)
		PC ← PC + $((\mathtt{disp}_{10})^5$ ## $\mathtt{disp}_{10..0})$;

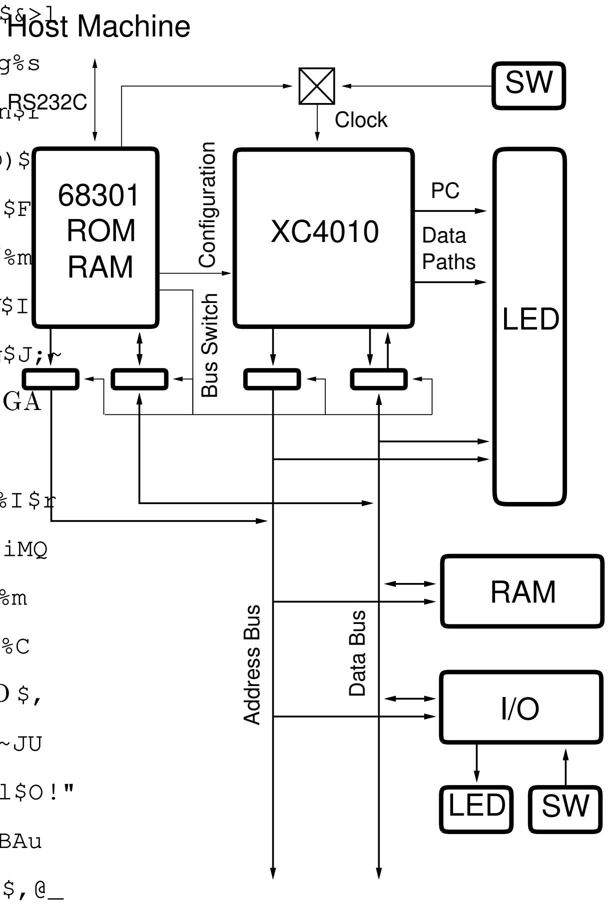
I= 4: @)8fL?Na

<L?? 1: %W%m%;%C%5%\!<%I $N304Q

4 <B83MQ%\!<%I

%^%$%/%m%W%m%;%C%53+H/<B83$r8Bil$?;~4VFb$K9TJ&>l9g$K:G$bLdBjKJkN$O!"FPGA $N%3%s%U%#%0%l!<%7%g%s%G!<%?$r:n@.8e!"<B:]$K%G!<%?$r FPGA $KE>Aw$7$FF0:n$I3NG'9k:n6HG"$k!#3X@8<+?H$,!"FPGA $*$h$S<~JU2sO)$%f%K%P!<%5%k4pHD>e$KH>EDIU$1$*$h$S%i%C%T%s%0$rMQ$$$F8=9kN,M}A[G"k,!"3Nh&$JJ}K!$G$O!"%^%$%/%m%m%;%C%5$N<BAu$N$_$Ji:!"30It%a%b%j!"F~=PNOAuCVJI<~JU2sO)$d!"F0:n3NG'$N$?$a$N%b%K%?5!G=$N<BAu$KB?Bg$J;~4VrMW9$k!#$^$?!"ITMQ0U$JEE8;G[@~Kh$j9b2A$J FPGA $rGK2u$9$k2DG=@-$b$"$k!#

$=$3$G!"$3li$N<BAu$r4JC12=9k$?$a$N<B83MQ%\!<%I$r:n@.7? (<L?? 1)!#?^ 4$K<($9h&$K!"$3$N%\!<%I$O650iMQ%^%$%/%m%W%m%;%C%5$rE>Aw9k FPGA G"$k XC4010!"%W%m%0%i%`3JG<MQ$N%9%?%F%#%C%/ RAM(64kbyte)!"F~NOMQ%9%$%C%A!"FbIt%G!<%?%Q%9/%W%m%0%i%`%+%&%s%?$N%b%K%?MQ LED $,Hw$(il$F$$$k!#=@Fp@-$rA}$9$?$a!"FPGA $N%T%s$H<~JU2sO)$N4V$K$O%i%C%T%s%0%]%9%H$,@_1ilF$$$k!#3l$O!"2sO)5,LO$KhCFO%T%sG[CV$r;XDj$9kH FPGA >e$K<BAu$G$-$J$$2DG=@-$,$"k?aG!"3N>l9g3X@8O=l>l,@_7W7?%^%$%/%m%W%m%;%C%5$N%T%sG[CV!"%b%K%?7?$$=PNO$K9g$o$;$F%i%C%T%s%0$r9T$J$&!#



?^ 4: %W%m%;%C%5%\!<%I

FPGA $N%3%s%U%#%0%l!<%7%g%s%G!<%?$H!"PICO <+$N%M
%W%m%0%i%`$O!"<B833+;O;~$KE>Aw9kI,MW$,$"$k!#$3$N
%G!<%?$H%W%m%0%i%`$r%[%9H%^%7%s$+$iD>@\E>Aw9k$?$a$K
%\!<%IKO RS232C %$%s%?%U%'!<%9$H!"3l$r@)8f$9$k16bit
CPU 68301 $,Ek:\$5lF$$$k!#3N CPU $O4JC1$J%b%K%?
%W%m%0%i%`$N@)8f2<$GF0:n$7!"FPGA $NF0:n8e!"RAM $NFb
MF$r3NG'$9k3HJI,G-$k!#

$^$?!"FPGA XN%/%m%C%/$O%9$$%C%A$rMQ$$$F<jF0$GM?$(
k3HbG-k7!"68301 $N%?%$%^=PNO$rMQ$$$FG$0U$N<~GH
?t$N?.9f$rM?$($k3HbG$-$k!#

5 3+H/<B83$N<B;\Nc

1994 G/EY!"7DXf5A=NBg3X$*$h$SEl5~9)2JBg3X$K$*$$$F!"%^
%$%/%m%W%m%;%C%5$N3+H/<B83$r9T$JC?!#0J2<K=$N7k2L$H!"
$=$lKh$jL@$i$+$KJC$?LdBjE@$r$"$2$k!#

5.1 3+H/<B83$N=g=x

<B83$O!"7DXf5A=NBg3X$G$OM}9)3XItEE5$9)3X2J 3 G/@8$rBP
>]$K=5 4 %3%^×3 =54V!"El5~9)2JBg3XGO9)3XIt>pJs9)3X2J
3 G/@8$rBP>]$K=5 3 %3%^×6 =54Vr+1F9TJC$?!#

O@M}9g@.KO NTT <R$N PARTHENON 2.2.1 $r!"G[CVG[
@~KO Xilinx <R$N XACT 5.0.0 $r!"$^$? PARTHENON $N
=PNO7A<0G"$k NLD 7A<0%U%!%$%k$+$i!"XACT $NF~NO7A<0
G"$k XNF %U%!%$%k$NJQ49$K NTT EAAw$7$9%F%`8&5f=j$N
nld_xnf 2.1b $r;HMQ$7$?!#$5iK!"A0=R$N FPGA $K XC4010
$r;HMQ$7$?<B83MQ%\!<%I$rMQ$$$F!"3+H/7?%^%$%/%m%W%m
%;%C%5$NF0:n3NG'$r9TJC$?!#

3+H/<B83$N%9%F%C%W$O0J2<NDLjG"$k!#

STEP1 %O!<%I%&%'%"5-=R8@8l SFL $N5-=RK!$r=,F@9k!#
%5%$%3%m%+%&%s%?$JIN4JC1$J=g=x2sO)$r5-=R$7!"F0:n%7
%_%e%l!<%? SECONDS $GF0:n$r3NG'9k!#5i$KO@M}9g@.
$r9T$J$$9g@.5l$?2sO)$r%W%j%s%H7F8!F$$9$k!#$3$N%9
%F%C%WGOHIrAH^$:!"3F0w$,$=$l$>$l$N5-=R$r9T$J$$!"F0
:n$r3NG'$9$k!#

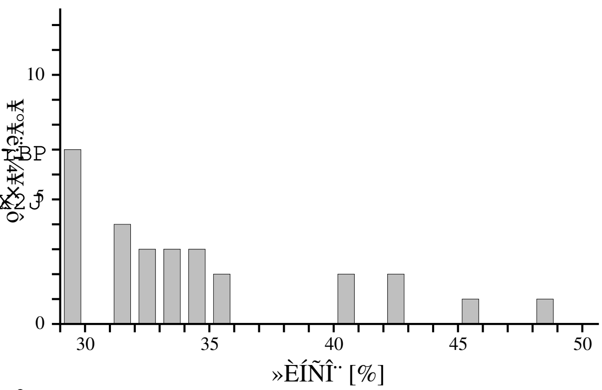
STEP2 BP>]H9$k%^%$%/%m%W%m%;%C%5 PICO $N35N,$K$D
$$$F@bL@$r<u$1!"HIKh$KL?Na%;%C%H$r7h$a!"J,C4$7$F5-=R$r
9TJ&!#;~4VE*@)Ls$+$i!"4pK\L?Na%;%C%H$N%3!<%G%#%s%0

N_$(!"<BAu$9Y-L?Na$bBeI=E*$J?t<o$K9J$C$?!#$?$@$
$,!"FPGA $N%5%$%:$,5v$98Bj5$^$6$^$J
$?$<BAu9k3H$,$G$-$k!#SECONDS >e$GA4$F$NL?Na$
$r3NG'$7$?CJ3,$G!"3N%9%F%C%W$r=*N;$9$k!#

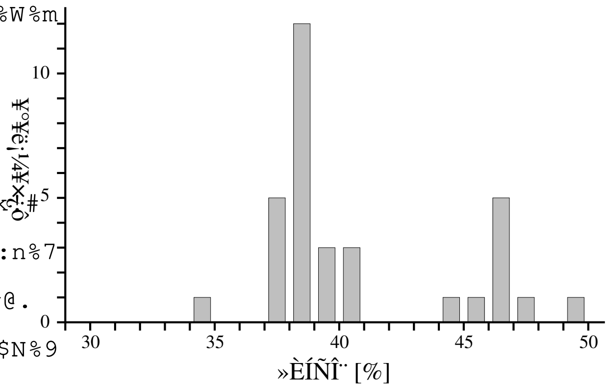
STEP3 O@M}9g@.!"%M%C%H%j%9%HJQ49!"Xilinx <R$N CAD
Kh$kG[CVG[@~$r9T$J$$!"%3%s%U%#%0%l!<%7%g%s%G!<%?$
@.$7!"$3lrA0=R$N<B83MQ%\!<%I$KE>Aw7FF0:n3NG'$r
J&!#=hM};~4V$N4X78$G!"G[CVG[@~$D!<%k$Khk%3%s%U%
%l!<%7%g%s%G!<%?XNJQ49$O!"=5$H=5$N4V$K<B83 T.A. $,
JCF*$/$N$,NI$$!#

5.2 3+H/<B83$N7k2L

:rG/EY!"9TJC$?<B83$N7k2L$+$i FPGA Cf$N function generator It$N;HMQN($r?^ 5$H?^ 6$K<($9!#



?^ 5: 7DXfBg3XK*1k FPGA $N;HMQN(



?^ 6: El5~9)2JBg3XK*1k FPGA $N;HMQN(

DN7k2L$+$i9M$($ilk3H$O!";~4VE*@)Ls$N87$7$$7
5A=NBg3XGO$[$\4pK\L?Na7+<BAuG-$F$$$J$$$NKBP
5l$F$$$k;~4V$KM>M5$N$"$kEl5~9)2JBg3XGO3X@8$N0UM_$r=

K~$?$7$F$$$kbN$H;W$olk!#CfKOL?Na$rDI2C$7$F$$$.$$!"

FPGA $K<}$^$j@Z$i$J$$%0%k!<%Wb"C?!#AJ$_$KA0=R$N XC4010 $N>l9g!";HMQ$G$-$k CLB(function generator) $N?t $O 800 G"$k!#

J*3N3+H/<B83$O 1995 G/EY$b9TJolF$*$j!"El5~9)2J Bg3XK*$$$F$O3XIt 2 G/<!8e4|$K3N<B83$G@_7W$9$k PICO-16 $rBj:`$K7W;;5!$N4pAC650i$r<x6H$G9T$J$&$3$H$K$h$j!"7W ;;5!%7%9%F%`$N014S7?650i$r<B8=$7$F$$$k!#

5.3 LdBjE@

<B83$N7P83$Khj0J2<$NLdBjE@$,L@i+KJC?!#

- O@M}9g@.!"G[CVG[@~$,3X@8$KHCFO$[$HsI%V%i%C%/%\%C%/%9G"$j!"$^$?$+Jj$N;~4V$rMW9k!#2a5nB`6~7F7^$&3X@8$,B?$+$C$?!#$AJ_$K!":G>.%;%C%H$N PICO-16(;HMQN(24%) GOG[CVG[@~$KLs 20 J,(SS10/SunOS5.3) $G=*N;$7$?$,!"%U%k%;%C%H$N PICO-16(;HMQN(89%) $@$HG[CVG[@~$K 2 ;~4V0J>e$+$+$C$?!#
- 0lEY$KB??t$NL?Na$r<BAu$7!"G[CVG[@~$NCJ3,$GF~j-iJ$/$JCF7^$&%0%k!<%W$,G?!#3N$?$a!"$;$C$+$/5-=R7?L?Na$r:o=|$9k3HKJj!"3X@8Ndk5$$rBg$$$K$=$$$G7^C?!#
- SFL $N5-=R$O!"%P%99=B$$,L@<(E*GJ$$!#3N$?$a!"3X@8$OL?Na$rIU$12C$($F$$$/:]$K!"D>@\%l%8%9%?$KBeF~9k5-=RrIsI$sA}$d7F7^$&!#$3Nh$&$J5-=R$O!"O@M}9g@.$GB?$/$N%^%k%A%W%l%/%5$rH/@8$5$;$k3HKJ$j!"Hf3SE*C1=c$JbNGb%A%C%W$KF~$j@ZiJ$/$JCF7^$&$3H,$"$C$?!#
- %P%9$K FPGA Fb$N 3 %9%F!<%H%P%C%U%!$r;HMQ$7h&$H;n$_$?$,!"%i%$%V%i%jEy$NITET9gKhj&$^$/;HMQG-J+C?!#3lKD$$$F$O8=:_:F8!F$CfG"$k!#
- I,MW%2!<%H?t$r8:$i9?aK FPGA $N%i%$%V%i%j$rMQ$$$h$&$H;n$_$?$,!"G[CVG[@~%D!<%k$NET9g$G<B8=$G$-$J$+$C$?!#$?$@$7 RAM N_$O2DG=$G$"$C$?$?$a!"FH<+$K PARTHENON MQ$N%i%$%V%i%j%U%!%$%k$r5-=R$7;HMQ$7$?!#

6 $*$ojK

Js9p7?<B83%7%9%F%`$NFCD9$NRHDO!"0B2A$KF3F~

$-$kE@K"$k!#<B83MQ%\!<%I<+BN$O!"FPGA $N2A3J$r4^$

20 K|1_A08e$G<B8=$G$-$k!#5i$KBg3X$G$O!"NTT <R$h$

PARTHENON $*$h$SJQ49$D!<%k$NL5=~B_M?$r<u1k3H$,

G-!"%i%s%K%s%0%3%9%HO[HsI+$+$i$J$$!#$^$?!"$

DxEYB?$/$N?M?t$rBP>]$H9k3H$,$G$-$k3H$+$i!"B?$

;dN)Bg3XGNF3F~$,2DG=$G$"$k$H;W$olk!#

7+$7!"$3$3$GHj$"$2$? PICO-16 $O%O!<%I%&%'%"5-=

8@8lGN5-=R$NMF0W@-$K94CF7^C?$?$a!"%W%m%;%C%

7F$OG<F@$Nf/%l%Y%k$^$GC#7J$+$C$?!#:#8e!"$5i

NI$r=E$M!"%Q%$%W%i%$%s2=!"%-%c%C%7%e%a%b%jEy$N7W;;5

0lMQ$N65:`$H7F!"$^$?!"%"%;%s%V%i%d%3%s%Q%$%i!"%A%

$7W$NINB>$N650i$HO"78$7$?bN$KH/E8$5$;$F$$$-$?$

<U<-

PARTHENON $r8fDs6!$$$?$@$$$? NTT <R!"$*$h$S%M%C

%H%j%9%H$NJQ49$D!<%k$rG[I[$7F/$@$5C?F1<REAAw%7%

%8%5%i=j$NE{0f>OGn;a$K46<U$$$?7^$9!#

$^$?!"3X@8<B83$N T.A. $rG.?4$KEXaF$$$?$@$$$?7DXf5

=NBg3XM}9)3XIt$N@> 9(>O;a!";3K\ =c;a!"9u_7 HtEMLp;a$

SKEl5~9)2JBg3X$N8eF# HK@8;a$K46<U$$$?7^$9!#:G8e$

G.?4$K<B83$r9TJCF/l?7DXf5A=NBg3XM}9)3XItEE5$9

2JJiSKEl5~9)2JBg3X9)3XIt>pJs9)3X2J$N3X@8=t7/$K4

7^$9!#

;29MJ88%

[1] <F;3 7i!"?7Ui <#CK, "Bg3XK*1k7W;;5!%"!<%-%F%

%A%c$N650iJ}K!$K4X9k9M;!", >pJs=hM}3X2q7W;;5!%"

%-%F%/%A%c8&Js 100-4, Jun. 1993.

[2] 1[CR!"_7ED!"2,ED!">eEh!"?@86!"_@8}!"0B1:, "7W;;5!9)3

=8@Q2sO)9)3X650iMQ%^%$%/%m%W%m%;%C%5 KUE-CHIP2",

3.3XJs CPSY92-47, Oct. 1992.

[3] 4d0fBt ?pJf B>, "7W;;5!9)3X014S650iMQ%^%$%/%m%W%

%;%C%5 QP-DLX $N3+H/", >pJs=hM}3X2q7W;;5!%"!<%-%F

%/%A%c8&Js 100-5, Jun. 1993.

[4] EDCf!">.1)ED!"5W2f!"Kv5H, "650iMQ%^%$%/%m%W%m%;%C

KITE H=$N3+H/;Y1g4D6-", >pJs=hM}3X2q7W;;5!%"!<%-%F%/%A%c8&Js 100-8, Jun. 1993.

[5] >>K\>0, "%W%m%;%C%5:n@.3X@8<B83-%A%C%W!"%\!<%I$+$i%3%s%Q%$%i!"%"%W%j%1!<%7%g%s$^$G", %^%$%/%m%(%l%/%H%m%K%/%98&5f3+H/5!9= Bh 12 2s%o!<%/%7%g%C%W%W%m%7!<%G%#%s%0 pp.1-12, Dec. 1993.

[6] CfB<9T9(!">.LnDj9/, "ULSI $N8z2LE*$J@_7WK!", %*!<%`<R, 1994.

[7] NTT %G!<%?DL?.3t<02q<R, "PARTHENON Reference Manual", NTT %G!<%?DL?.3t<02q<R, 1989-1990.

[8] NTT %G!<%?DL?.3t<02q<R, "PARTHENON User's Manual", NTT %G!<%?DL?.3t<02q<R, 1989-1990.

[9] Xlinx Inc., "The XC4000 Data Book", Xlinix Inc., 1991.

[10] J.L.Hennessy, D.A.Patterson, "Computer Architecutre: A Quantitative Approach", Morgan Kaufmann Pub. Inc., 1990.