AN ASYNCHRONOUS SWITCHING FABRIC

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Abstract— A simple switching fabric which works completely in an asynchronous manner without a system clock was implemented. It is equipped with 4 input/output ports, each of which has 4-bit data width. Though the 0.6-micrometer conservative CMOS process is used, an original circuit design achieves 7.4Gbit/s per a port and 29.6Gbit/s/chip in the simulation. Now, the chip is operational, and achieves 3.2Gbit/s/chip bandwidth on a test board.

I. Introduction

In order to cope with wiring delay and clock skew problems on recent advanced VLSI chips, asynchronous design which does not require a common clock is one of the hopeful ways. It is also advantageous for low power consumption and availability in various environments compared with common synchronous designs.

Although several researches have been exerted for designing general asynchronous processors[1][2], few works[2] have been done on asynchronous component architectures. In this paper, an important component, a switching fabric, is implemented completely in asynchronous manner.

II. Chip Features

The switching fabric chip is designed according to the following policies:

- Both the chip operation and input/output signals are completely designed in an asynchronous manner.
- The bandwidth in the burst mode was given the top priority in optimization.

The total asynchronous design makes the arbiter circuits simple. While traditional synchronous arbiter requires complicated circuits like the round robin priority controller for the fairness, the asynchronous arbiter just selects the fastest request. Thus, the operation speed is much improved.

For a high bandwidth burst communication, an input port keeps holding the communication path to an output port once it gets the right until the requester releases it. Since the communication path consists of simple gates: a 3-input NAND, two NOT gates, a 2-input NAND and a 2-input AND, the low latency signal transmission is possible without disturbing the shape of waveform.

III. Circuits

The implemented switching fabric is divided into the following four major parts:

1. head of line conflict detection,
2. arbiter,
3. output port selection, and
4. output port.

The head of line conflict detection part checks whether there are requests to the same output port. When it founds them, the circuit asserts a signal to the arbiter. In the arbiter shown in Fig.1, the delay element is adjusted so as to change the input requesting signal and the head of line conflict existing signal at the same time on inputs of the AND gate.

The output is kept H-level from the time when a request is accepted until it is released, that is, during the output port is allowed to use.

4 by 6 3-input NAND gates matrix negates the corresponding output that satisfies the following conditions:

- The signal from output selection is asserted, thus the output is selected.
- The signal from arbiter is asserted, thus the input wins.
- Input data is asserted.

The output port multiplexes the signal from the input port.

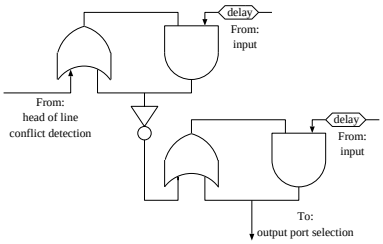

Fig. 1.: arbiter

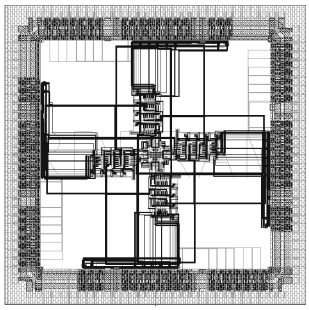

Fig. 2.: layout

IV. Implementation

The chip consists of the above described circuits and handshake circuits which inform the conflict to sender. In this chip, it is assumed that gates consisting of an identical layout have the same delay parameter. And a bundled-data asynchronous data transfer is adopted in order to reduce the number of signals. The number of input/output ports and bit width of each port are also decided mainly with the pin limitation of the chip. As a result, 4 input/output ports each of which consists of 4-bit bundle data are provided.

The full custom layout shown in Fig.2 is done with LayoutPlus editor supported by VLSI Design and Education Center(VDEC).

Here, Rohm's 0.6-μm CMOS process supported by VDEC program is used. The number of gates normalized 2-input NAND gates is 1030, and the total area of the chip is $21.16mm^2$.

V. Simulation

At first we show the results of circuit level simulation using HSPICE according to extracted parameters from the layout. Through the simulation, the maximum transfer rate is evaluated as 29.6 Gbit/s/chip in the burst mode. (Fig.3)

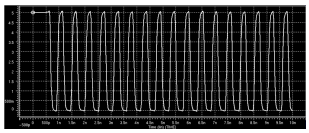

Fig. 3.: simulation signal wave(0ns-10ns,0v-5V)

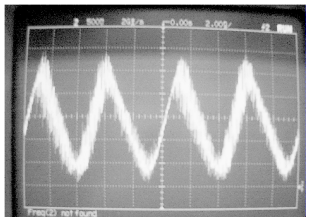

Fig. 4.: Signal wave (0v-2v)

VI. Evaluation of the real chip

A simple board was developed to evaluate the real chip, and the initial evaluation results are as follows.

- It takes 10 - 12 ns to establish the path and to start transfer.
- It takes 6 - 8 ns as the data transfer latency.
- Although the input signal frequency is limited with the current test board, the maximum transfer rate that we can measure is 3.2 Gbit/s/chip in the burst mode. Fig.4 shows the transferred signal on an output port.

VII. Conclusion

Fully asynchronous controlled switching fabric is implemented. It could transfer 29.6 Gbit/s/chip maximums in the burst mode in simulation. It worked correctly, and it could transfer 3.2Gbit/s/chip actually at least.

References

[1] Akihiro Takamura,Masashi Kuwako,Masashi Imai,Taro Fujii,Motokazu Ozawa,Izumi Fukasaku,Yoichiro Ueno,Takashi Nanya, "TITAC-2:An asynchronous 32-bit microprocessor based on Scalable-Delay-Insensitive model," *International Conference on Computer Design(ICCD)*, October, pp. 288-294, 1997.

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