

7 MOPS/lemon-battery image processing demonstration with an ultra-low power reconfigurable accelerator CMA-SOTB-2

Main objectives and topics

Cool Mega Array (CMA)-SOTB-2 is an energy efficient reconfigurable accelerator for recent advanced sensor networks, Internet of Things and wearable computing. It is implemented by using Silicon on Thin BOX (SOTB) CMOS technology developed by the Low-power Electronics Association & Project (LEAP). Compared to the previous prototype, the CMA-SOTB which we showed a demonstration with a solar battery in FPL 2014, it is optimized to achieve sufficient performance with a extremely limited power budget. In order to demonstrate its performance with an extremely small power, this year, we will try to execute a simple image processing application (Alpha-blender) with 7 MOPS performance by the lemon battery.

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1 Introduction

Cool Mega Array (CMA)-SOTB-2 is an ultra-low energy Coarse Grained Reconfigurable Architecture[1] (CGRA) for recent advanced sensor networks, Internet of Things and wearable computing. It has a large Processing Element (PE) array without memory elements for mapping an application's data-flow graph, a small simple programmable μ -controller for data management, and data memory. Unlike traditional coarse grained reconfigurable processors, the power consumption for hardware context switching, storing intermediate data in registers, and clock distribution for them are eliminated from PE array which occupies large area of a chip. It is implemented by using Silicon on Thin BOX (SOTB) CMOS, a new process technology developed by the Low-power Electronics Association & Project (LEAP).

2 CMA-SOTB-2

Figure 1 shows a block diagram of the CMA-SOTB-2 architecture. In order to improve the energy efficiency of the previous prototype, the CMA-SOTB, the performance of μ -controller is improved by introducing parallel data memory access with data manipulators, and optimization of both instruction set and micro-architecture. A delay learning mechanism which finds the optimal delay time for the computation in the PE array is also introduced.

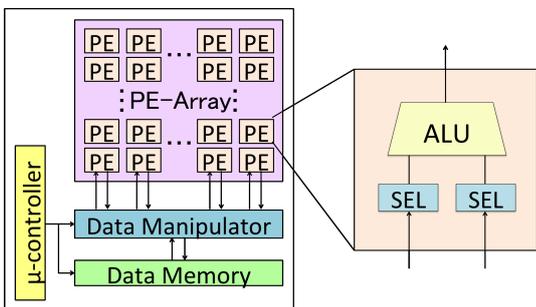


Figure 1: Block diagram of the CMA-SOTB-2

3 SOTB CMOS technology

The silicon on thin buried oxide (SOTB)[2] is a novel fully depleted SOI CMOS technology developed by the Low-power Electronics Association & Project (LEAP). In SOTB, transistors are formed on thin buried oxide layer as shown in Figure 2. By using SOTB, extensive body (back-gate) bias control is applied to optimize the performance and leakage power consumption after fabrication.

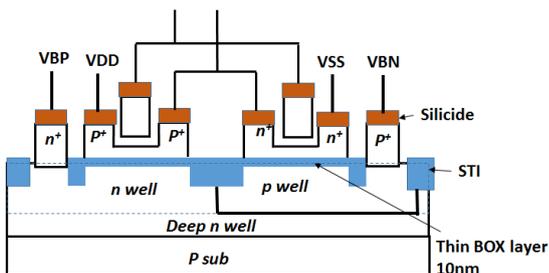


Figure 2: Cross sectional view of the SOTB Device

4 Evaluation

Figure 3 shows the performance of the three simple image processing programs at various supply voltages. Dashed lines show the MOPS/mW at each application without the body bias control, and solid lines show the best MOPS/mW when the energy efficiency was optimized by the body bias control. A 743 MOPS/mW sustained performance was achieved with 0.4 mW at 0.5 V supply voltage.

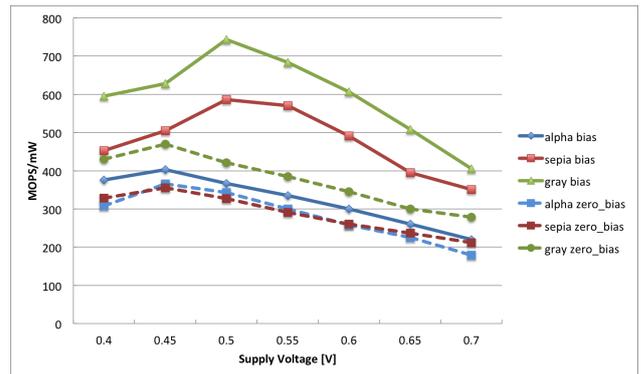


Figure 3: Performance vs supply voltage by application programs

5 Demonstration

The CMA-SOTB-2 is especially useful when the supply energy budget is limited or energy harvesting battery with a large internal resistance is used. Figure 4 is a photo of the CMA-SOTB-2 executing *alpha* at 7 MOPS with a lemon battery using six pieces. A piece of lemon generates about 0.7 V but the internal resistance is large, about 1.5K Ω . Thus, a strong reverse body bias is given so that it works with an extremely low current 0.37 mA. It also works with the solar battery under the room light.

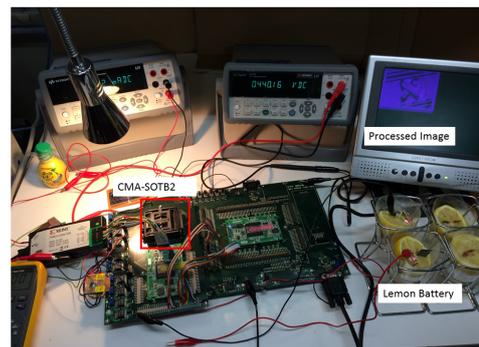


Figure 4: Demonstration of CMA-SOTB-2 using lemon battery

References

- [1] N.Ozaki, et al. "Cool Mega-Arrays: Ultralow-Power Reconfigurable Accelerator Chips", *IEEE MICRO*, 6–18, 2011.
- [2] H.Su, et al. "Body bias control for a coarse grained reconfigurable accelerator implemented with Silicon on Thin BOX technology", *Field Programmable Logic and Applications (FPL) 2014*, 1–6, 2014