Curriculum Vitae

2014.
Hideharu Amano

Short Biography

Hideharu Amano received the Ph.D degree from Keio University, Japan in 1986 under Prof. Hideo Aiso's supervision.. From 1985, he was a research associate of department of electric engineering, Keio University. He studied in Stanford University CSL from 1989-1990 as an Assistant Professor. He joined Prof. Tobagi's project to develop a high speed multi-stage interconnection network. From 1991, he was an associate Professor of information and computer science, Keio University. From 2001, he has been a full professor of the same department.

Research Projects

High Performance Parallel Machines

He developed a shared memory with snoop cache like communication memory called $(SM)^2$. It was presented in ISCA in 1983 and 1985. He also developed a multiprocessor with a high performance interconnect called SNAIL in 1993. He joined Japanese national project by Ministry of Education and developed JUMP-1 from 1995-2000. Also, he joined a Real World Computing project and developed RHiNET-2 from 2000-2005. His projects include interconnection or middleware of clusters using GPUs. He joined to CREST project from 2012, and has been working to develop a low-latency switching system using PCIe with University of Tsukuba and The University of Tokyo.

Interconnection Networks

One of his continuous research subject is interconnection networks. He proposed various novel networks, Recursive Diagonal Torus, Piled Banyan Switching Fabrics, Fault Tolerant Batcher network, and Folded-Fat Torus with his students and colleagues. His friends to discuss this subject is Dr. Koibuchi of NII, Dr. Matsutani of Keio University and sometimes Prof.Hsu of Fordham University.

Dynamically Reconfigurable Devices

He started his WASMII project from 1992, and proposed multi-context style dynamic reconfiguration. It was one of roots of current dynamically reconfigurable processors. He made a co-research project with NEC electronics and contributed to develop their DRPs. Now, he is working for his own chips called MuCCRA, and MuCCRA-3 with e-shuttle 65nm and MuCCRA-4 with ST micro 28nm are available.

Low Power Computation

In the Ultra-Low Power System project in CREST from 2006, he is now working with Prof.H.Nakamura of Univ. of Tokyo, Prof.M.Namiki of Tokyo University of Agriculture and Technology, Prof.K.Usami of Shibaura Institute of Technology, Prof.M.Kondo, Tokyo Electro-Communication Univ. and Prof.Kuroda of Keio Univ. With them, he developed a low power accelerator Cool Mega Array-1/2 and a micro-processor with fine-grained power gating Geyser-1/2.

Building Block Computing System

He started Kakenhi-S (National fund from JSPS) project from 2013. The subject is establishment of building block computing systems in which each computing element is connected with wireless inductive coupling link. This project is also done with Prof. Kuroda, Prof. Usami, Prof. Namiki, Prof. Kondo, Prof.Nakamura and Prof.Matsutani.

Contribution

He was a head of technical group of computer systems, IEICE from 2011-2013. He also a SC member of ICFPT and ARCS. In 2009, he was a PC Chair of ICFPT, and General Chair in 2013. He is one of funders of HEART, and was General Chair in 2012 and 2014. He has been an OC vice chair of CoolChips from 2010-2014, and also was/is a PC member of IPDPS, FPL, ICFPT, RAW, MWSCAS and ReConfig. He was an editor of Journal of Parallel and Distributed Computing until 2013, and now an editor of IEICE Transaction and ACM Transaction on Reconfigurable Technology and Systems.

Journal Papers (Since 2000)

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