Parallel Programming Contest2019
HLS Section

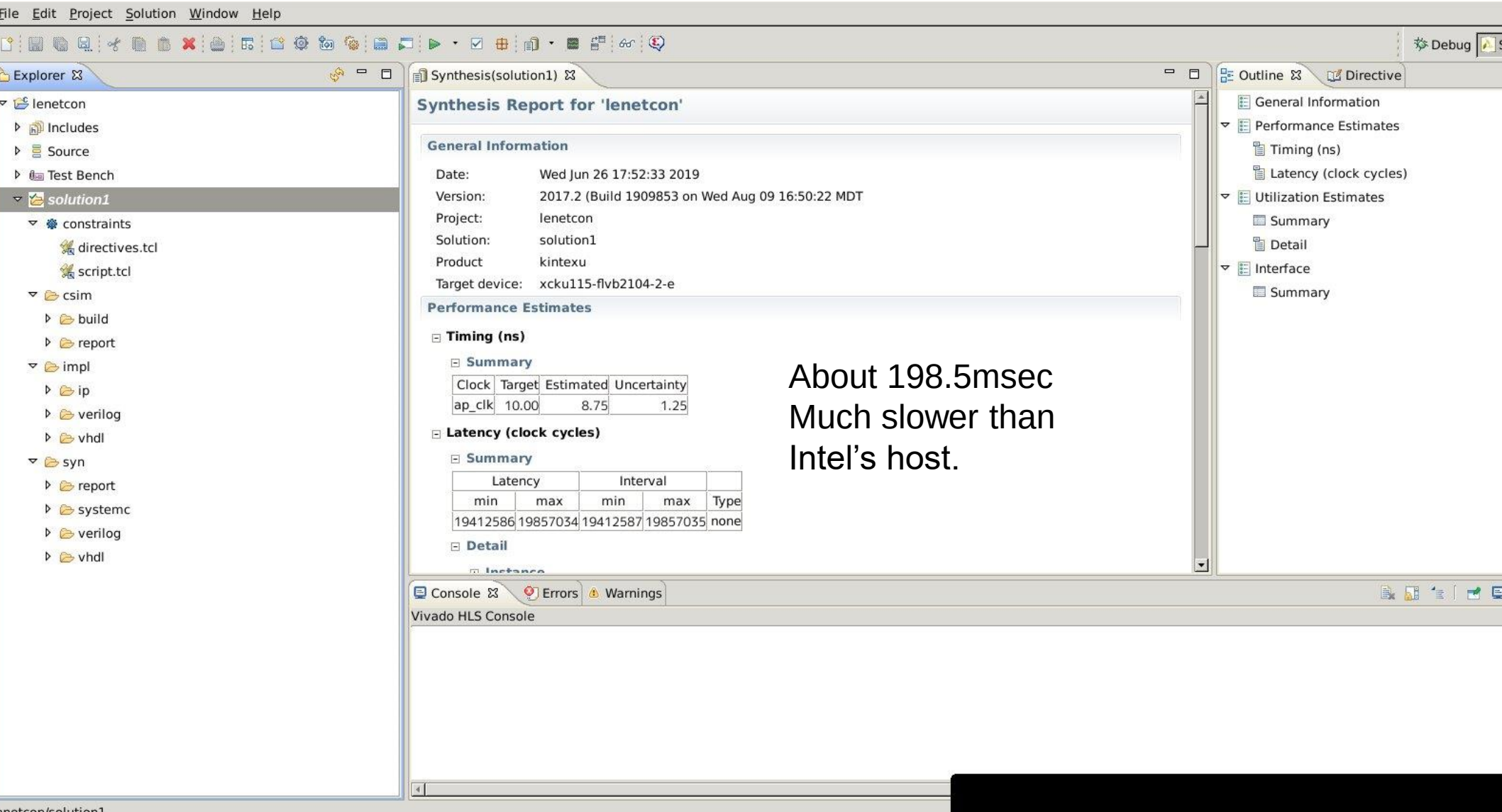
A simple CNN: LeNet
Get lenet_fpga from the web site.

1. HLS optimization

- Download con19.tar.gz from the website.
- tar cvf con19.tar.gz or archive manager will take care.
- cd con19/lenetcon
- vivado_hls
  - open project -> ./lenetcon/lenetcon
  - Place con19 on your home directory.
  - Don’t change the hierarchy.

Optimization

- Use techniques in “Vivado_HLS.pptx”.
- Of course, you should check Xilinx’s web site.
- Synthesize and check the results.
  - All resources should be within 60% to avoid long implementation time.
- Make sure your original design must generate the same results.
- After optimization, execute “Export RTL”.
- Then exit vivado_hls.


File Edit Project Solution Window Help
Debug
Explorer
lenetcon
Includes
Source
Test Bench
solution1
constraints
directives.tcl
script.tcl
csim
build
report
impl
ip
verilog
vhdl
syn
report
systemc
verilog
vhdl
Synthesis(solution1)
Synthesis Report for 'lenetcon'
General Information
Date: Wed Jun 26 17:52:33 2019
Version: 2017.2 (Build 1909853 on Wed Aug 09 16:50:22 MDT
Project: lenetcon
Solution: solution1
Product kintexu
Target device: xcku115-flvb2104-2-e
Performance Estimates
Timing (ns)
Summary
Clock Target Estimated Uncertainty
ap_clk 10.00 8.75 1.25
Latency (clock cycles)
Summary
Latency Interval
min max min max Type
19412586 19857034 19412587 19857035 none
Detail
About 198.5msec
Much slower than
Intel's host.
Outline
Directive
General Information
Performance Estimates
Timing (ns)
Latency (clock cycles)
Utilization Estimates
Summary
Detail
Interface
Summary
Console
Errors
Warnings
Vivado HLS Console

ndow Help

Debug Synthesis Analysis

Synthesis(solution1) lenetcon_csim.log

```
  isize=800, osize=500

ReLu:
  isize=1, ichan=500

Classifier:
  isize=500, osize=10

Softmax:
  isize=10

    0 : 0.000000
    1 : 0.000000
    2 : 0.000000
    3 : 0.000017
    4 : 0.000000
    5 : 0.000000
    6 : 0.000000
    7 : 0.999978
    8 : 0.000000
    9 : 0.000005
total error=0
 GO HLS FEEDFORWARD
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] **************** CSIM finish ****************
```

total error=0 must be shown up

Outline Directive

An outline is not available.

Console Errors Warnings

Vivado HLS Console

```
    9 : 0.000005
total error=0
 GO HLS FEEDFORWARD
INFO: [SIM 211-1] CSim done with 0 errors.
INFO: [SIM 211-3] **************** CSIM finish ****************
Finished C simulation.
```

timer

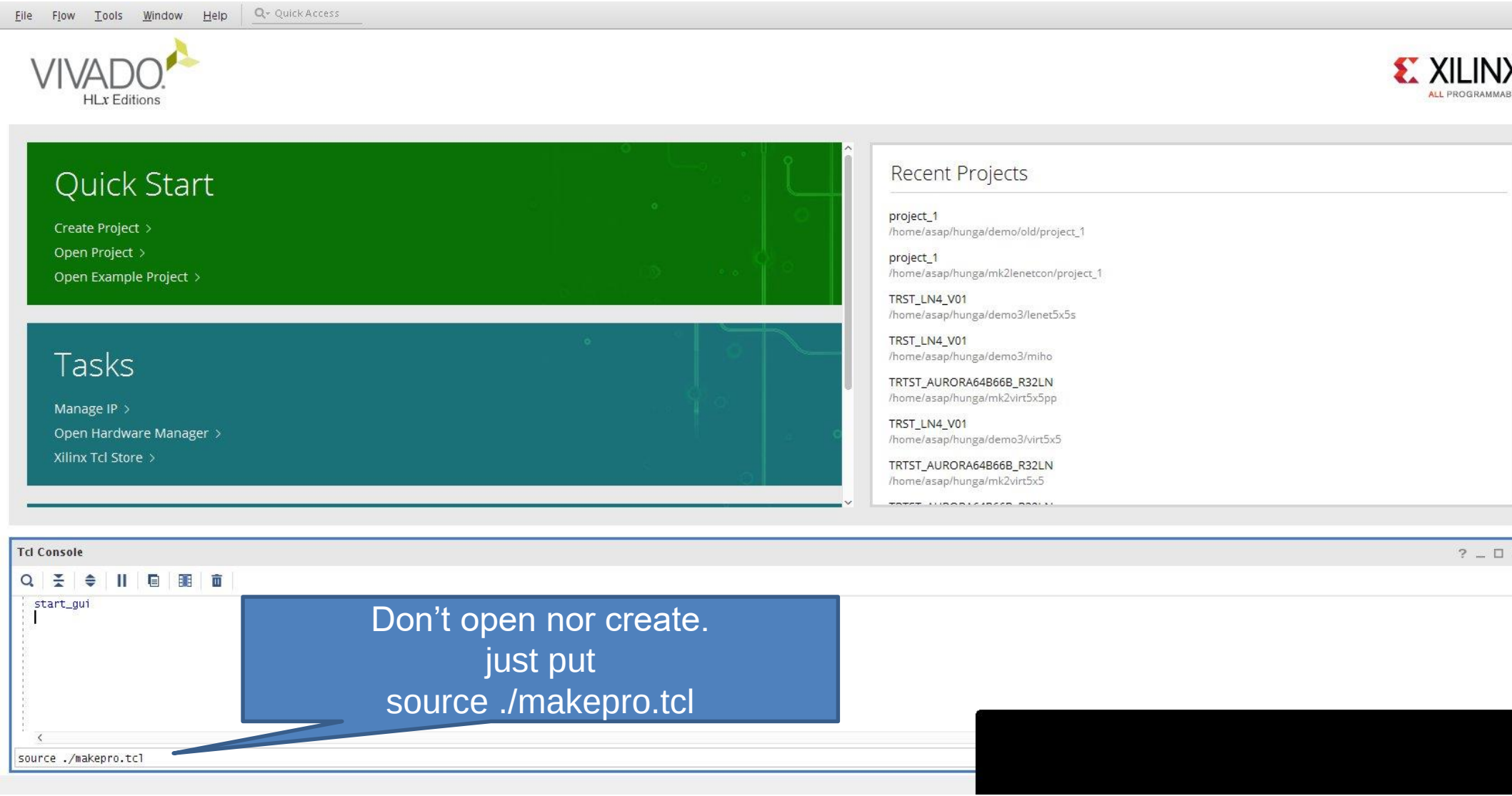
- C simulation does not accept the timer control.
- In lenetcon.c activate
  statt[0] = 1; before convl, and
  stopt[0] = 1: after fc2

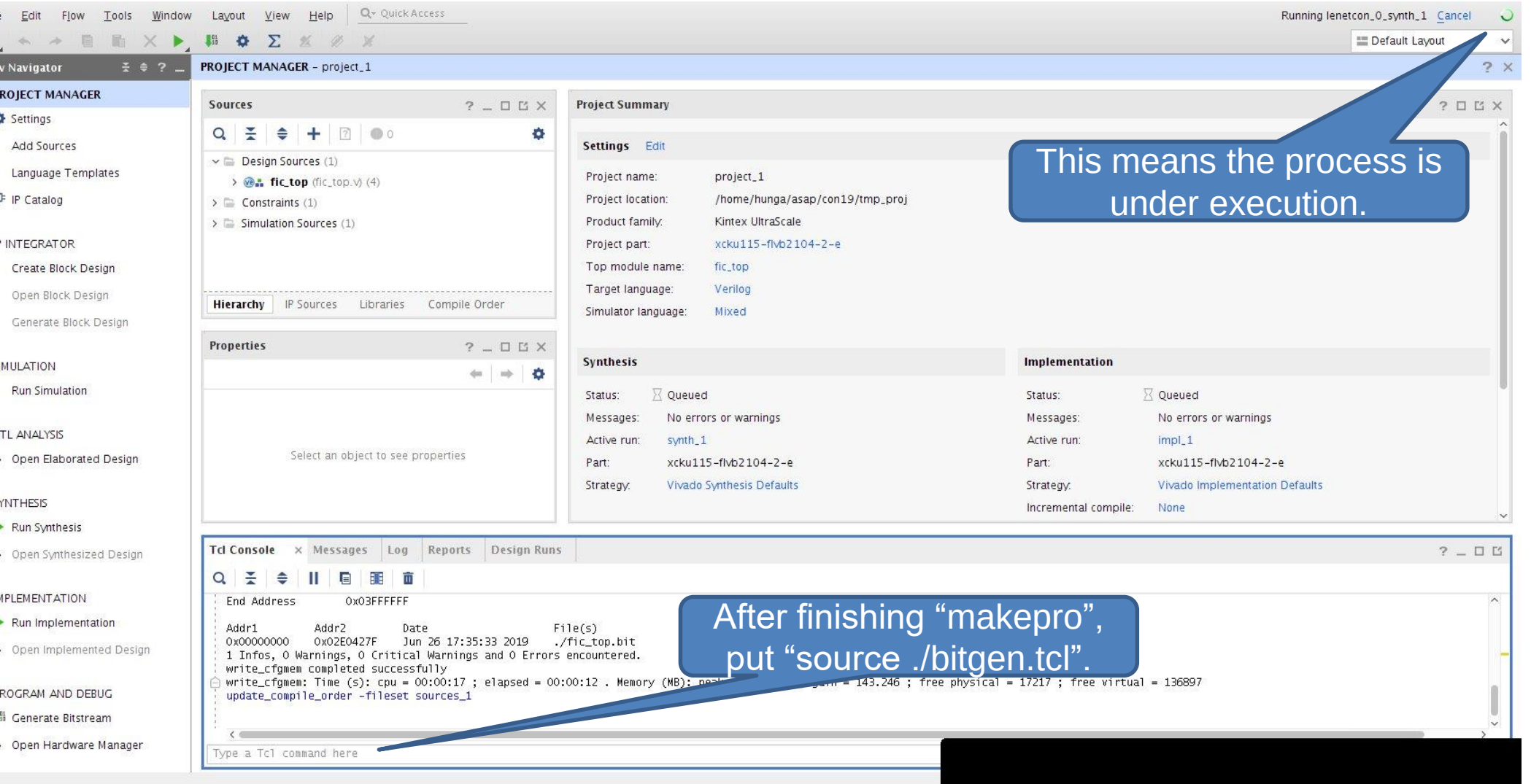
Then, synthesyze.

Now, this problem has been fixed by using #ifdef __SYNTHESIS__

2. FPGA design by Vivado

- Arrange “makepro.tcl” for your environment.
  /home/md401/aa85035/con19-> Your home directory/con19
- /bin/rm –rf tmp_proj
  - Make sure there is no tmp_proj directory when you apply the script.
- vivado
  - Put “source ./makepro” in the tcl window
  - If there is no problem, all processes will be done automatically.
    - It will take about 20 mins. for the base design.
    - If your design is big, it sometimes takes a day.
    - “Bitstream Generation successfully completed” window will pop up.
  - After clicking “Cancel”, put “source ./bitgen.tcl”.
  - fic_top.bin, the configuration bit is generated.
  - File-> Exit
- Caution! vivado/vivado_hls requires a large disk space.


File Flow Tools Window Help
Quick Access
VIVADO
HLx Editions
XILINX
ALL PROGRAMMAB
Quick Start
Create Project >
Open Project >
Open Example Project >
Tasks
Manage IP >
Open Hardware Manager >
Xilinx Tcl Store >
Recent Projects
project_1
/home/asap/hunga/demo/old/project_1
project_1
/home/asap/hunga/mk2lenetcon/project_1
TRST_LN4_V01
/home/asap/hunga/demo3/lenet5x5s
TRST_LN4_V01
/home/asap/hunga/demo3/miho
TRTST_AURORA64B66B_R32LN
/home/asap/hunga/mk2virt5x5pp
TRST_LN4_V01
/home/asap/hunga/demo3/virt5x5
TRTST_AURORA64B66B_R32LN
/home/asap/hunga/mk2virt5x5
Tcl Console
start_gui
Don’t open nor create.
just put
source ./makepro.tcl
source ./makepro.tcl

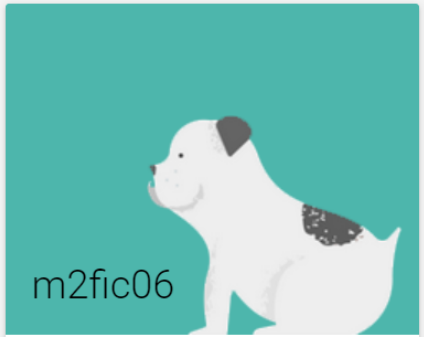

Edit
Flow
Tools
Window
Layout
View
Help
Quick Access
Running lenetcon_0_synth_1
Cancel
Default Layout
Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
MULATION
Run Simulation
TL ANALYSIS
Open Elaborated Design
YNTHESIS
Run Synthesis
Open Synthesized Design
MPLEMENTATION
Run Implementation
Open Implemented Design
ROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_1
Sources
Design Sources (1)
fic_top (fic_top.v) (4)
Constraints (1)
Simulation Sources (1)
Hierarchy
IP Sources
Libraries
Compile Order
Properties
Select an object to see properties
Project Summary
Settings
Edit
Project name: project_1
Project location: /home/hunga/asap/con19/tmp_proj
Product family: Kintex UltraScale
Project part: xcku115-flvb2104-2-e
Top module name: fic_top
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Queued
Messages: No errors or warnings
Active run: synth_1
Part: xcku115-flvb2104-2-e
Strategy: Vivado Synthesis Defaults
Implementation
Status: Queued
Messages: No errors or warnings
Active run: impl_1
Part: xcku115-flvb2104-2-e
Strategy: Vivado Implementation Defaults
Incremental compile: None
This means the process is under execution.
Tcl Console
Messages
Log
Reports
Design Runs
End Address 0x03FFFFFF
Addr1 Addr2 Date File(s)
0x00000000 0x02E0427F Jun 26 17:35:33 2019 ./fic_top.bit
1 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_cfgmem completed successfully
write_cfgmem: Time (s): cpu = 00:00:17 ; elapsed = 00:00:12 . Memory (MB): peak
= 143.246 ; free physical = 17217 ; free virtual = 136897
update_compile_order -fileset sources_1
Type a Tcl command here
After finishing “makepro”, put “source ./bitgen.tcl”.

3. Execute on the FPGA

- You need your account on zeus@am.ics.keio.ac.jp
- Send the name if you try to join the FPGA section to yasuaki@am.ics.keio.ac.jp
- ssh –Y zeus@am.ics.keio.ac.jp
- Start firefox and check the website: http://www.am.ics.keio.ac.jp/fic-management-system
- Reserve vacant machine from m2fic08-m2fic11

hlab FiC Management System

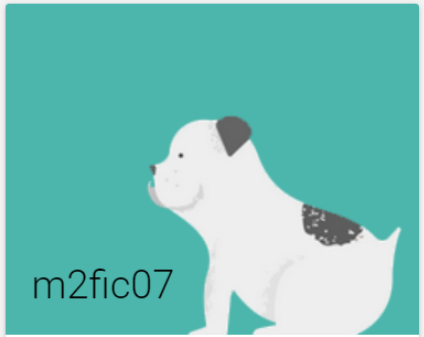
You are logged in as Hideharu Amano LOGOUT



User

Memo

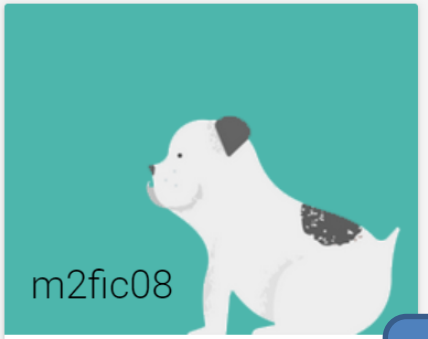
Board ID



User

Memo

Board ID

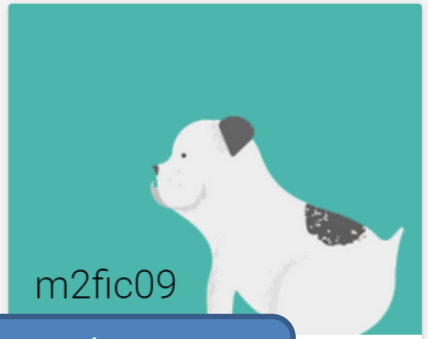


User
hunga

put your name here

Memo

Board ID



Memo

Board ID

Script arrangement

- scp your fic_top.bin and test.sct.
- Arrange the path for test.sct.
  - You must use the absolute path.
- ./test.sh
- The configuration and execution are automatically done.

test.sh

This must be your fic_top.bin file

This must be your reserved fic board

#

/home/asap/fic/ras_hunga/ficmgr.py -t m2fic08 -p /home/hunga/asap/con19/fic_top.bin –pm sm16

/home/asap/fic/ras_hunga/ficmgr.py –t m2fic08 –runcmd “/home/hunga/asap/con19/rasbpi/remote" --runcmdtimeout 5

Read the timer (Ignore the first one)

Flow-in-Cloud (FiC) SW Board

FiC Network
8x4 9.9Gbps

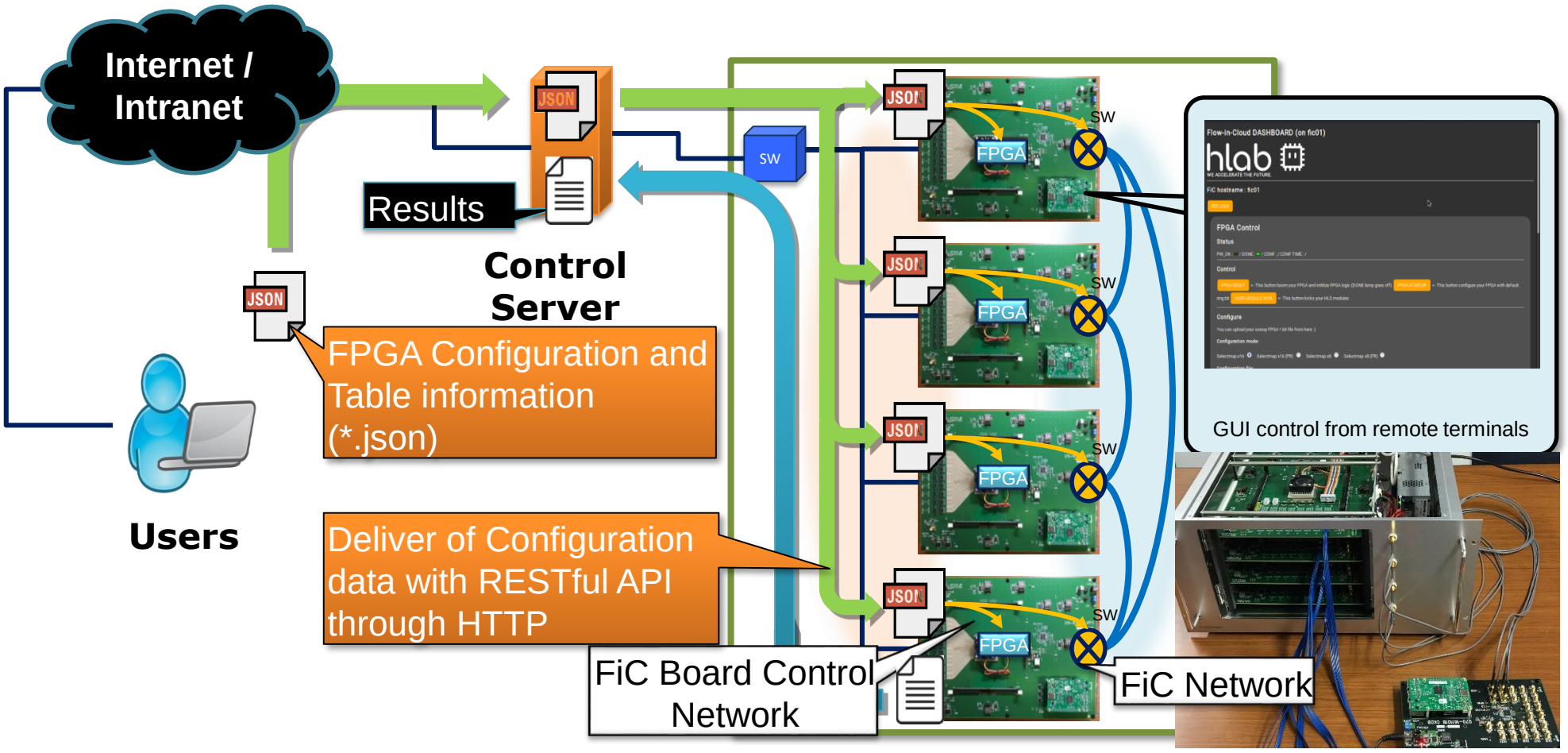
Here, we call each
link “channel”,
and a bundle of
4 channels “bundle”.

A board has 8 bundles
each of which has
4 channels

Ethernet

Control Network

The current FiC system



Report

- Leave your design in “lenet” directory in your home directory.
- Send the mail to hunga4125@gmail.com with a report and your account number.
- The result must be the same as the current version.
- The deadline is 8/2 24:00. Never delayed.
- The ranking will appear on the web site.
- If you have any question, mail to yasuaki@am.ics.keio.ac.jp.