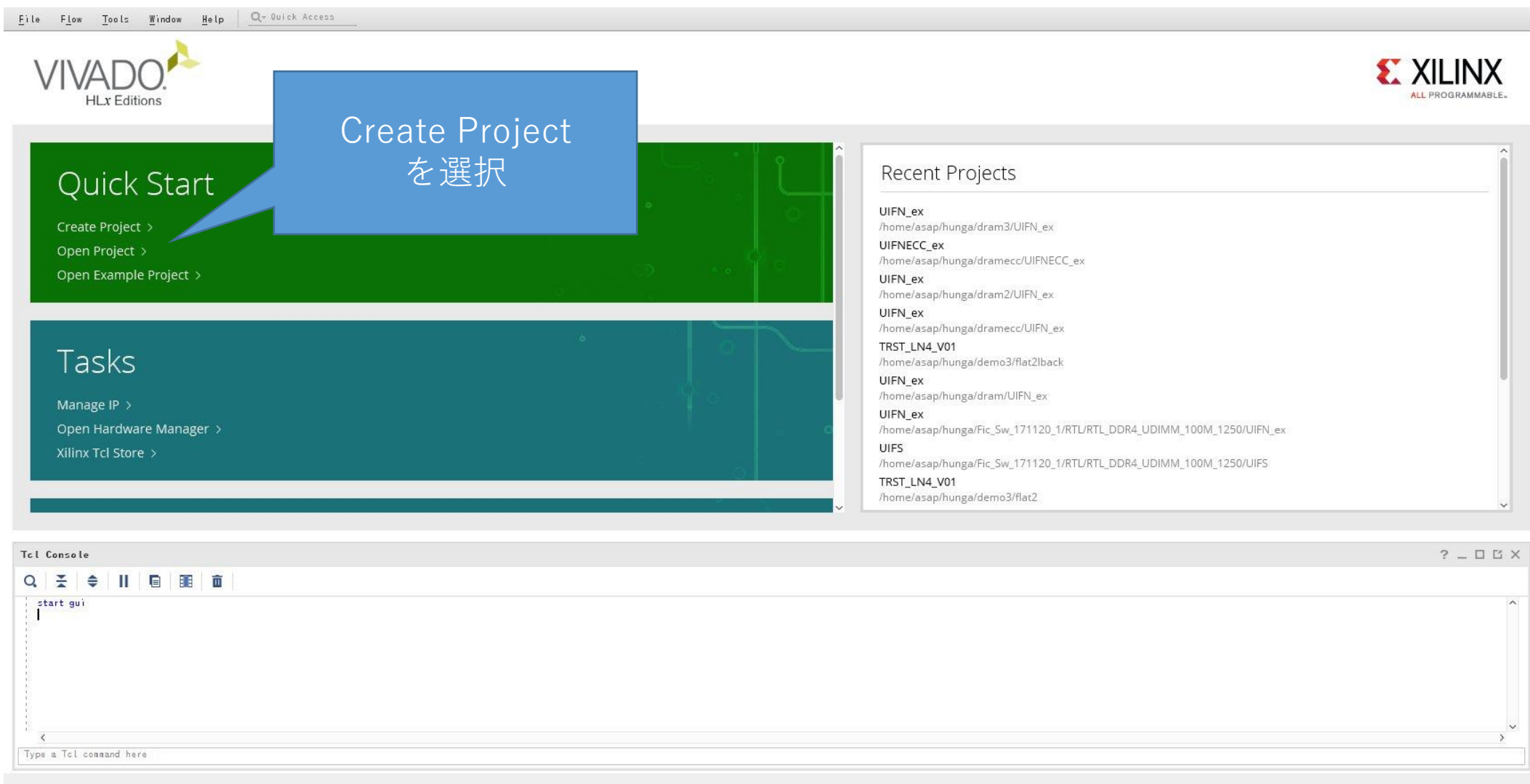


VivadoでPOCOを合成する

マイクロプロセッサ特論

天野

vivadoと打ち込み立ち上げる



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: /home/hunga/verilog/code/synthvivado/p

プロジェクトのサブディレクトリを作成

プロジェクト名はproject_1でOK

locationはsynthvivadoにしておく

Next



< Back

Next >

Finish

Cancel

+ を クリ ッ ク

表れたファイルを
全部選択
→OK

NEXT

Create File

☐ Copy sources into project

Target language: Verilog

Simulator language: **Mixed**

②

[← Back](#)

[Next >](#)

Finish

Cancel

Constraint fileはpoco.xdcを選択
OK→Next

Look in: synthvivado

project_1
poco.xdc

poco.xdc中にはclkを10nsec (100MHz)に設定してある

Recent Directories

/home/hunga/verilog/code/synthvivado

File Preview

```
create clock -period 10 [get nets clk]
```

File name: poco.xdc

Files of type: Design Constraint Files (.sdc, .xdc)

OK

Cancel

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.



Select: ☒ Parts ☐ Boards

Filter

Product category: Speed grade:

Family: Temp grade:

Package:

Reset All Filters

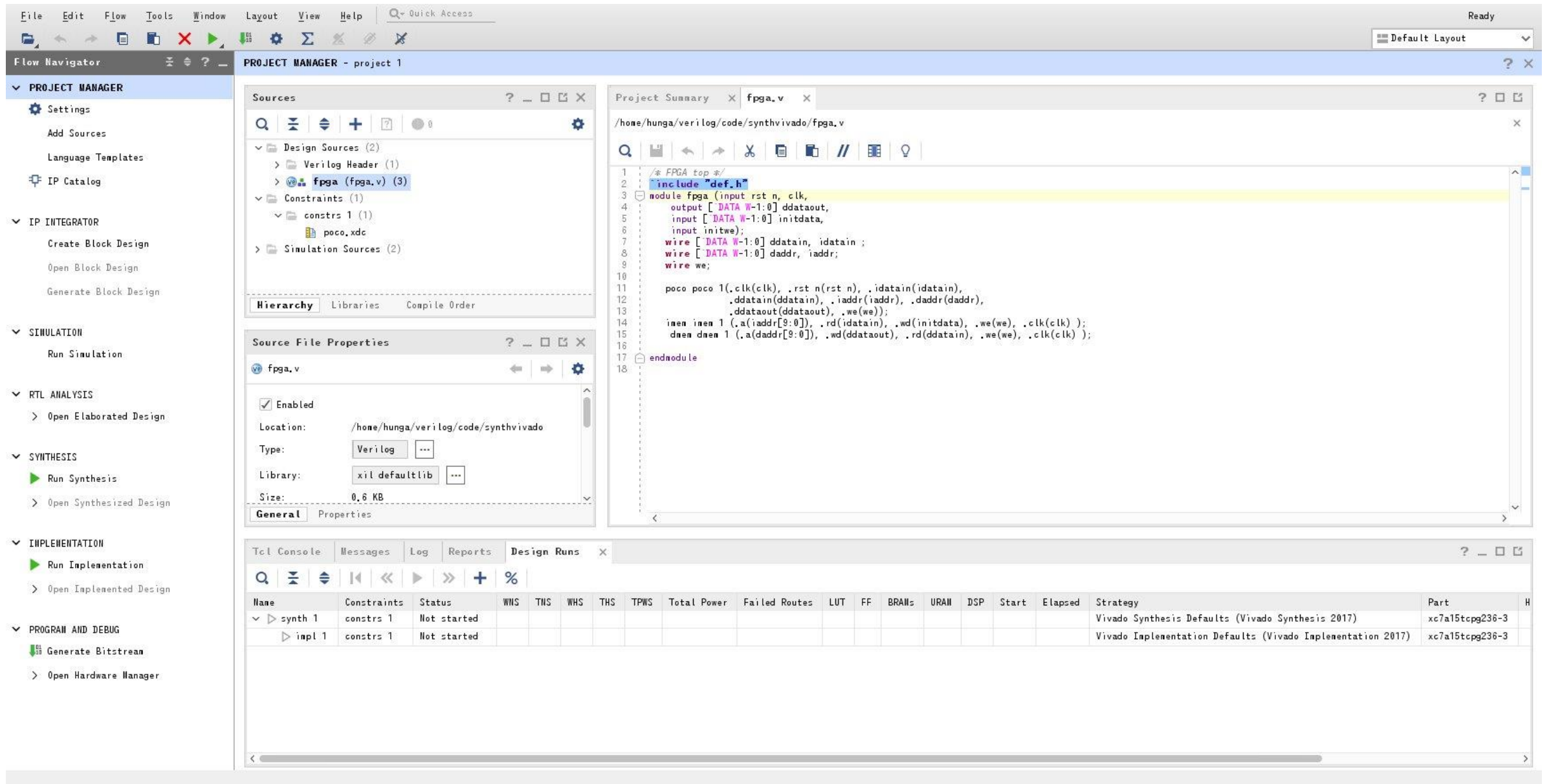
Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceivers
☒ xc7a15tcpg236-3	236	106	10400	20800	25	0	45	2	2
☐ xc7a15tcpg236-2	236	106	10400	20800	25	0	45	2	2
☐ xc7a15tcpg236-2L	236	106	10400	20800	25	0	45	2	2
☐ xc7a15tcpg236-1	236	106	10400	20800	25	0	45	2	2
☐ xc7a15tcsg324-3	324	210	10400	20800	25	0	45	0	0
☐ xc7a15tcsg324-2	324	210	10400	20800	25	0	45	0	0
☐ xc7a15tcsg324-2L	324	210	10400	20800	25	0	45	0	0
☐ xc7a15tcsg324-1	324	210	10400	20800	25	0	45	0	0
☐ xc7a15tcsg325-3	325	150	10400	20800	25	0	45	4	4
☐ xc7a15tcsg325-2	325	150	10400	20800	25	0	45	4	4
☐ xc7a15tcsg325-2L	325	150	10400	20800	25	0	45	4	4
☐ xc7a15tcsg325-1	325	150	10400	20800	25	0	45	4	4



デバイスの選択
Artix-7a15tcpg236-3にしておく
Artix-7aの中では小さいが、
16640Logic Cell
900KbのBRAMを持つ

FamilyをArtix-7を選択
xc7a15tcpg236-3を選択
Next→Finish



プロジェクトの画面： Run Synthesis（論理合成）→Run Implementation（配置配線）

File Edit Flow Tools Window Layout View Help Quick Access

Implementation Complete ✓
Default Layout

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC

IMPLEMENTED DESIGN - xc7a15tcbg236-3 (active)

Sources Netlist

- fpga
 - Nets (226)
 - Leaf Cells (35)
 - dmem 1 (dmem)
 - imem 1 (imem)
 - poco 1 (poco)

Source File Properties

fpga.v

Enabled

Location: /home/hunga/verilog/code/synthvivado

Type: Verilog

Library: xil_defaultlib

General Properties

Project Summary Device x fpga.v

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.440 ns	Worst Hold Slack (WHS): 0.124 ns	Worst Pulse Width Slack (WPWS): 3.950 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 5136	Total Number of Endpoints: 5136	Total Number of Endpoints: 657

All user specified timing constraints are met.

Timing Summary - impl 1 (saved)

Implementation終了後、Open Implementationを行った図、Deviceの様子が見れる

File Edit Flow Tools Window Layout View Help Q Quick Access Implementation Complete

Flow Navigator

- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION**
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic

IMPLEMENTED DESIGN - xc7a15tcbg236-3 (active)

Sources Netlist x

- fpga
 - Nets (226)
 - Leaf Cells (35)
 - daen 1 (daen)
 - inen 1 (inen)
 - poco 1 (poco)

Source File Properties

fpga.v

Enabled

Location: /home/hunga/verilog/code/synthvivado

Type: Verilog

Library: xil_defaultlib

General Properties

Project Summary x Device x fpga.v x

Incremental compile: None

DRC Violations

Summary: 2 critical warnings, 1 warning

Implemented DRC Report

Timing Setup | Hold | Pulse Width

Worst Negative Slack (WNS): 0.44 ns

Total Negative Slack (TNS): 0 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 5136

Implemented Timing Report

Utilization Post-Synthesis | Post-Implementation

Graph | Table

LUT 7%

LUTRAM 5%

FF 1%

IO 32%

BUFG 3%

Utilization (%)

Power Summary | On-Chip

Total On-Chip Power: 0.116 W

Junction Temperature: 25.6 °C

Thermal Margin: 74.4 °C (14.7 W)

Effective θ_{JA} : 5.0 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Implemented Power Report

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

- Check Timing (33)
 - Intra-Clock Paths
 - Inter-Clock Paths
 - Other Path Groups
 - User Ignored Paths

Timing Summary - impl 1 (saved)

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.440 ns	Worst Hold Slack (WHS): 0.124 ns	Worst Pulse Width Slack (WPWS): 3.950 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 5136	Total Number of Endpoints: 5136	Total Number of Endpoints: 657

All user specified timing constraints are met.

Project Summaryをクリック：Timing, Utilization, Powerが表示される。
詳細が見たい時はTools→Reportをクリック

レポートの見方

- Timing : FPGAの動作タイミング
 - Total Negative Slack (TNS) が0nsecになっていれば目標達成、この場合は100MHzで動作する
 - 制約が満足できないと赤字で出る
- Utilization: FPGAのリソース利用率
 - LUT : Look Up Tableでランダムロジック 7 %
 - LUTRAM: LUTで作ったRAM 5 %
 - FF: CLB中のFlip Flop 1 %
 - I/O : I/Oピン 32 %
 - BUFG:バッファ 3 %
- Total On-Chip Power: 目安

演習

- 制約ファイルを書き換えて5nsにしてやってみよ。
- その時のTNSを報告せよ。
- LUTの%は変化したか？

メール中のテキストデータで報告せよ。