1. Overview

Recent mobile computing systems provide wireless communication feature.
- Battery driven: power-aware system is essential
- Signal-to-Noise ratio (SNR) will vary dynamically
- Bit Error Rate (BER) must be kept for service quality
- The system should be optimized for the circumstances

Adaptive Computing with a dynamically reconfigurable device:
Hardware structure is dynamically reconfigured so as to reduce power consumption or enhance the performance of error correction

→ Adaptive Viterbi Decoder Design

2. DRP-1 Architecture

DRP is a coarse-grained dynamically reconfigurable processor architecture released by NEC electronics in 2002.
- A DRP-1 is the first silicon implementation of DRP architecture
- The basic building unit called Tile has 8-bit 8x8 processing element (PE) array and distributed memory modules
- PE operations and inter-PE connections can be dynamically changed by the instruction called Context
- Context switching can be performed cycle by cycle based on simple state transition diagram

3. Viterbi Algorithm

The Viterbi is the maximum likelihood decoding alg. for a class of error correcting technique known as convolutional coding.
- Size of Trellis Diagram: $2^{K-1} \times 5(K-1)$
- Error correction capability is depending on Constraint Length $K$
- If the large $K$ is selected, we will gain
  - High error correction capability
  - Large circuits, large power, and low-speed decoding

→ Trade-offs

Adaptive Computing with DRP-1:
- If the high error correction is required, the powerful design will be selected.
- In the case of good condition, changing to the design with lower error correction will reduce the power

4. Adaptive Viterbi Decoder

Five Viterbi decoders with $K = 3, \ldots, 7$ are implemented, and optimal design will be chosen according to the target SNR.
- The Viterbi Decoder Designs:
  - Systolic array structure
  - 1-bit Hard Input and 1-bit Hard Output
  - Code rate = $1/2$
  - Trace back length = $5(K - 1)$

Implementation onto DRP-1:
- Context data set of 5 Viterbi decoders are cached in the single DRP-1 device
- By switching the context, the design will be also switched in one clock cycle

5. Performance and Cost Evaluation

Evaluation Environment:
- The pseudo input bit sequences including certain bit errors are generated on the host PC
- The input bit sequences are transferred to the DRP-1
- The results are returned to the host PC and verified

Performance Results (Normalized to $K = 3$):
- Operational units: 269 \(\rightarrow\) 3201
- Power Consumption: 428.9 \(\rightarrow\) 1028.9 [mW]
- SNR (BER=10\(^{-5}\)) = 5.3dB \(\rightarrow\) 3.2dB
- Throughput: 9.95 \(\rightarrow\) 4.71 [Mbps]

Adaptive Computing Impact:
- Noise model: Log-distance pass loss model
- Practical measurement results of cities in Germany [Sei91] (pass loss exponent $n = 2.7$, std. deviation $\sigma = 11.8$dB)
- If the gain is 50dB, power can be saved up to 58.3%