MAPLE chip: a processing element for a static scheduling centric multiprocessor

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Abstract— A custom processor called MAPLE which supports static scheduling by automatic parallelizing compilers is implemented and evaluated. MAPLE has a high performance floating point arithmetic unit and fast data transfer mechanism between other MAPLE chip. The maximum operational frequency of MAPLE chip is 80MHz in simulation, and the operation on the prototype board with 23MHz clock is confirmed. Its required power consumption is about 0.56W at 23MHz operation.

I. Introduction

Although it is easy to enhance the peak performance of the multiprocessor only by adding many processing units, it is difficult to exploit effective performance for users without support of automatic parallelizing compilers. However, such compilers have been tailored for existing multiprocessors which are designed without care of them well. The multiprocessor system ASCA(Advanced Scheduling oriented Computer Architecture)[1] has been proposed based on the idea that not the parallelizing software is tailored for machines, but a multiprocessor system should be designed to make the best use of parallelizing software.

In ASCA, a multi-grain parallelizing compilation scheme[2] is adopted. The scheme can exploit parallelism of the user program in various levels of granularity: coarse-grain parallelism (macro-data flow computation), medium-grain parallelism (loop-level parallelism) which is used in most of the current compilers, and near-fine-grain parallelism (statement level parallelism). Since the near-fine-grain parallelizing compilation especially requires a precise static scheduling between operations, uncertain behavior of the processor must be completely excluded. To solve the problem, we have proposed the custom processor MAPLE[1](Multiprocessor system ASCA Processing eLEment).

II. Chip Features

MAPLE is a 32-bit RISC processor which provides a simple structure with highly predictable operations. Its instruction set is an extension of that of DLX[3]. Five-stage pipeline structure of MAPLE is designed to execute every operation in a fixed number of clocks. A floating-point execution unit[4] includes 32-bit/64-bit IEEE std 754-1985 floating-point unit.

There are 32 integer registers and 32 floating point registers. Furthermore 16 32-bit special registers called receive registers for fast data transfer between other MAPLE chip are provided.

The receive register is directly connected to MAPLE pipeline ID stage, and when the source processor executes a transfer operation between registers, data is directly sent out from the MEM stage of the pipeline. The transferred data is also directly received by a receive register of destination processor.

Fig. 1 illustrates the data transfer between other MAPLE chip by using receive registers.

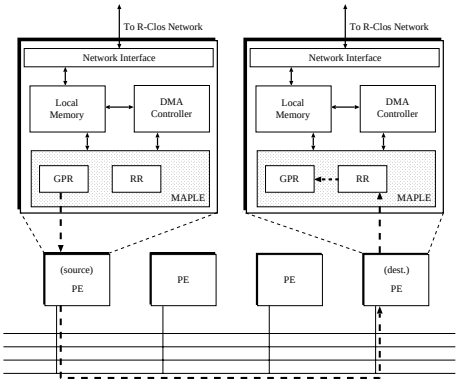

Fig. 1. Data Transfer with Receive Register(RR)

III. Implementation

The MAPLE chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

The chip specification and required gates are shown in Table I and Table II. The static delay path analysis results show that the operational frequency of this MAPLE chip is 80MHz. Fig. 2 shows its layout and the packaged die.

TABLE I
The Specification of MAPLE

Technology	Die size	Package
Rohm CMOS 0.35μm Std.Cell Poly 2, Metal 3, Vdd=3.3V	14.2mm $\times$ 14.2mm	PGA 572pin

TABLE II
NUMBER OF GATES

Module	Number of Gates
Integer Unit	21,486
Floating Unit	145,745
Receive Register	5,254
Others	1,525
Total	174,010

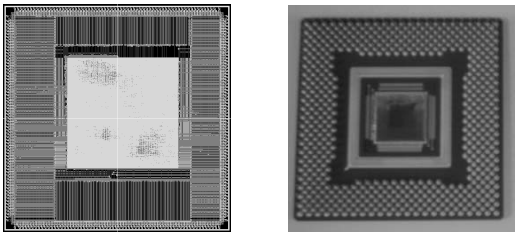

Fig. 2. The MAPLE Cell Layout and packaged Die

IV. EVALUATION

A. Prototype PE board

A prototype PE (Processing Element) board with the MAPLE chip is developed as a target of near-fine grain scheduling (Fig. 3). It provides software cache control system, 512k-byte main memory, 32kbyte instruction RAM, 32kbyte flash ROM, and a serial interface. When the system is starting up, a monitor program in the flash ROM runs. Under the management of the monitor program, the user program code is loaded from host computer through the serial interface, and executed.

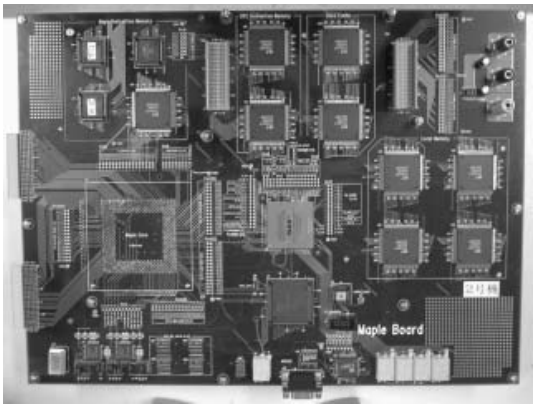

Fig. 3. Prototype PE board

This board is operational at 23MHz clock which is much less than 80MHz which is the target frequency of the MAPLE chip. The main reason of the frequency degradation is that the I/O pins assignment error was found after the board fabrication, and the MAPLE chip is mounted on a large daughter board for replacing the pin connections, which introduces various electronic problems.

B. Performance

The performance of the MAPLE chip with 23MHz clock is evaluated by π-series-calculation which includes 30,000 iterations, and shown in Table III. For the comparison, the execution result with UltraSPARC-II, which is a chip with similar level of technology, is also shown in the table. While the application runs, the MAPLE chip requires 0.56W power consumption.

TABLE III
EVALUATION OF π-SERIES-CALCULATION

CPU	Clock rate[MHz]	Time[ms]	Cycles
Sun UltraSPARC-II[a]	296	48.6	14,385,600
MAPLE[a]	23	750.0	17,250,264

[a] OS:SunOS 5.8, Compiler:gcc 2.95.3, Compile Option:-O3
[b] Compiler:gcc 2.7.2.3, Compile Option:-O3

The MAPLE chip is designed as a PE for multiprocessor, and we found out that the performance of 4 PEs as 1 cluster is about 2.25 times higher than that of single PE[5]. So, if the MAPLE chip works 80MHz clock as designed, and runs with 4 PEs, the execution time becomes 95.8ms, 7.83 times better than the result in the table, and comparable to UltraSPARC-II.

V. CONCLUSIONS

The MAPLE chip is an element processor for a static scheduling centric multiprocessor multiprocessor ASCA. Although the performance is lower than UltraSPARC-II, the number of gates and power consumption of the MAPLE chip is so small that the cost/performance and power/preformance of the MAPLE cluster has possibility to contend with the recent supersclar processors.

ACKNOWLEDGEMENTS

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