Ultra Low Power Reconfigurable Accelerator CMA-SOTB-2

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1 Introduction

Cool Mega Array (CMA)-SOTB-2 is an energy efficient reconfigurable accelerator for battery driven device to realize low power and high performance processing. It has a large Processing Element (PE) array without memory elements for mapping an application's data-flow graph, a small simple programmable μ-controller for data management, and data memory. Unlike traditional coarse grained reconfigurable processors, the power consumption for hardware context switching, storing intermediate data in registers, and clock distribution for them are eliminated from PE array which occupies large area of a chip. And it is implemented by using Silicon on Thin BOX (SOTB) CMOS technology. SOTB is a new process technology developed by the Low-power Electronics Association & Project (LEAP).

2 CMA-SOTB-2

CMA-SOTB-2 is a coarse grained reconfigurable accelerator using SOTB technology. Figure.1 shows block diagram of the CMA-SOTB-2 architecture.

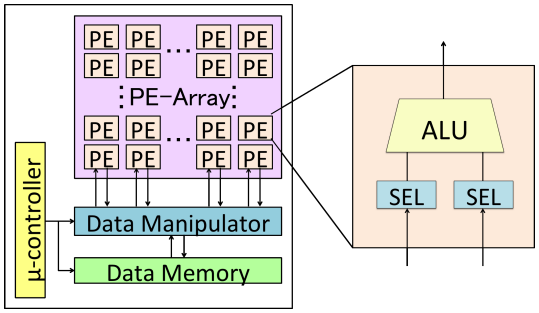

Figure 1: Block diagram of the CMA-SOTB-2

It consists of a large PE array consisting of combinational circuits, a simple programmable μ-controller which manages the data transfer between PE array and Data Memory and a Data Manipulator which controls the data from Data Memory to each PEs flexibly.

3 SOTB technology

SOTB is a new type of silicon on insulator (SOI) developed by Japanese national project LEAP. SOTB transistor is formed on thin berried oxide. Figure.2 shows cross sectional view of the SOTB transistor.

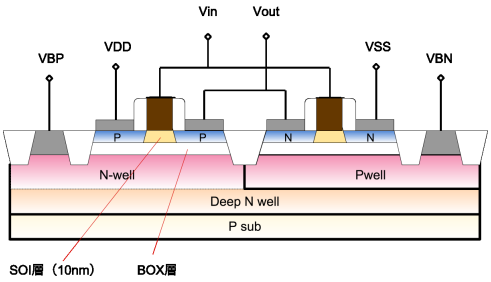

Figure 2: Cross sectional view of the SOTB Device

Since its characteristics variability is small, it can run at high speed with low supply voltage. Also its leakage power and delay can be widely controlled by body bias, so the performance balance can be controlled.

4 Evaluation

The performance by unit of power of the 3 application programs at various supply voltages is shown in Figure 3. These applications are simple image processings which are applied to input RGB data compressed into 24 bits. Dashed line shows the MOPS/mW at each application without body bias, and solid line shows the best MOPS/mW when the performance was controlled by applying body bias.

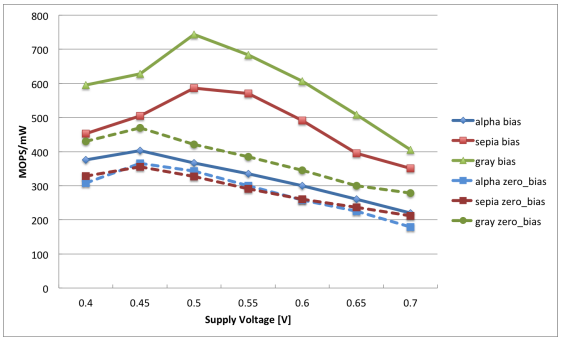

Figure 3: Performance vs supply voltage by application programs

When the supply voltage was 0.45V, 470MOPS/mW sustained performance was achieved at gray filter without applying body bias. Also when the performance was controlled by applying body bias, 743MOPS/mW sustained performance was achieved with supply voltage of 0.5V and power consumption of 0.4mW.

5 Demonstration

An image processing application (Alpha-blender) works on CMA-SOTB-2 at 25MHz with only 0.4-0.5V by the solar battery. Also it works at 5MHz with 0.8V by the lemon battery.

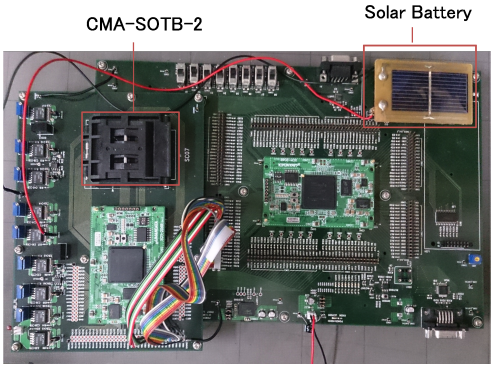

Figure 4: Demo board of CMA-SOTB-2

6 Conclusion

CMA-SOTB-2, a low power reconfigurable accelerator for embedded system, was implemented by using SOTB technology. It achieved high energy efficiency: 743MOPS/mW (297MOPS/0.40 mW) with a supply voltage of 0.5V.

References

[1] N.Ozaki, et al. "Cool Mega-Arrays: Ultralow-Power Reconfigurable Accelerator Chips", *IEEE MICRO, 6–18, 2011.*

[2] H.Su, et al. "Body bias control for a coarse grained reconfigurable accelerator implemented with Silicon on Thin BOX technology", *Field Programmable Logic and Applications (FPL) 2014, 1–6, 2014*